MB185Y IDTV
SERVICE MANUAL

Table of Contents

IMPORTANT

Before removing the rear cover from the TV for servicing, make sure that no cables are fixated to the cover. Release the cables from their clamps and disconnect (if any). Failure to do so may damage the wires and/or other components of the TV.

1. INTRODUCTION

17 MB185Y main board is driven by MTK SOC. This IC is a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high performance AV CODEC and CPU.

This board can be driven 50Hz UHD panels.

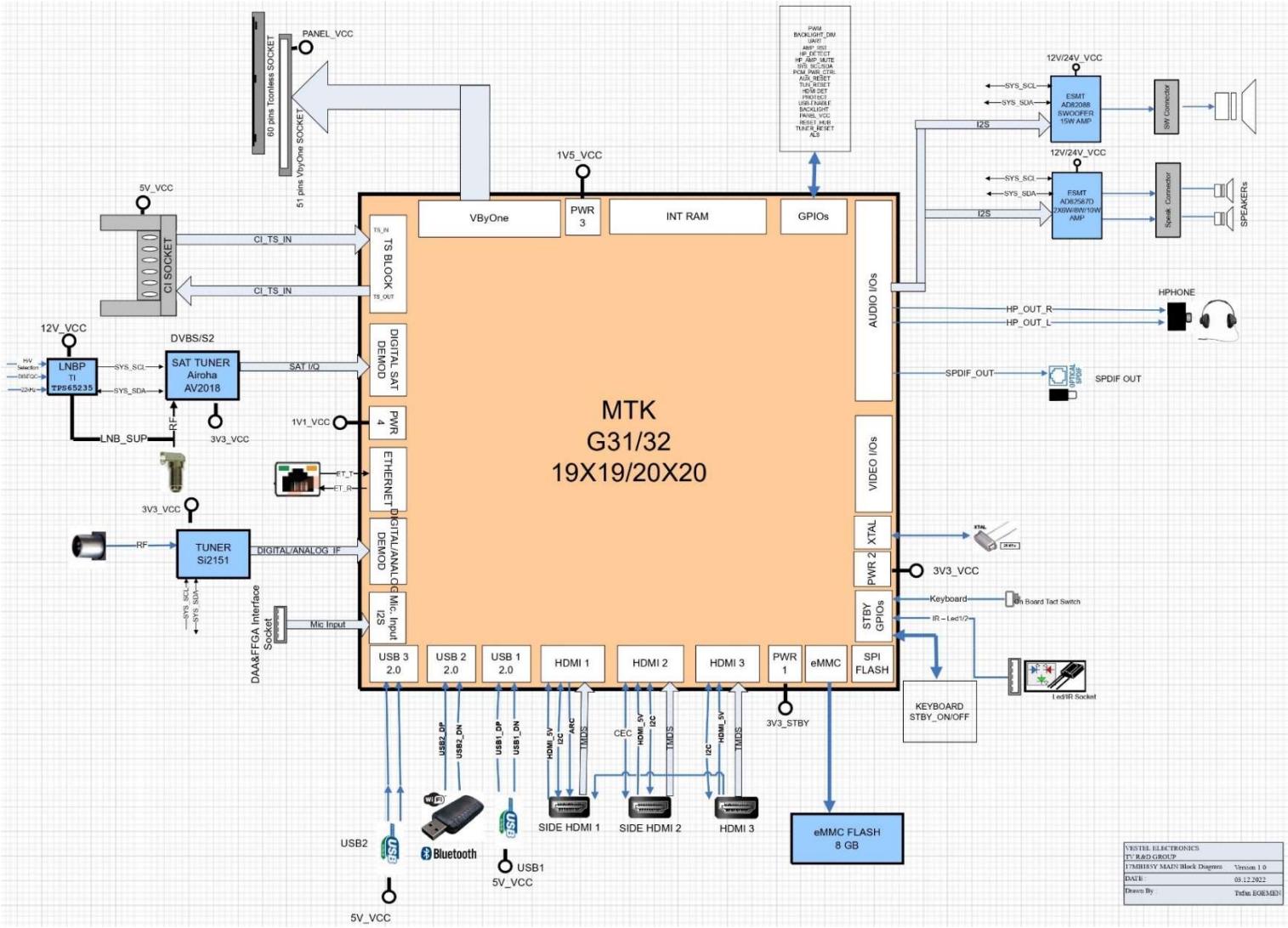
Key features include:

- Combo Front-End Demodulator
- A multi standart A/V format decoder
- The MACEpro video processor
- Home theatre sound processor
- Rich internet connectivity and completed digital home network solution
- Dual-stream decoder for 3D contents
- Multi-purpose CPU for OS and multimedia
- Peripheral and power management
- Embedded DRAM (for connected option)

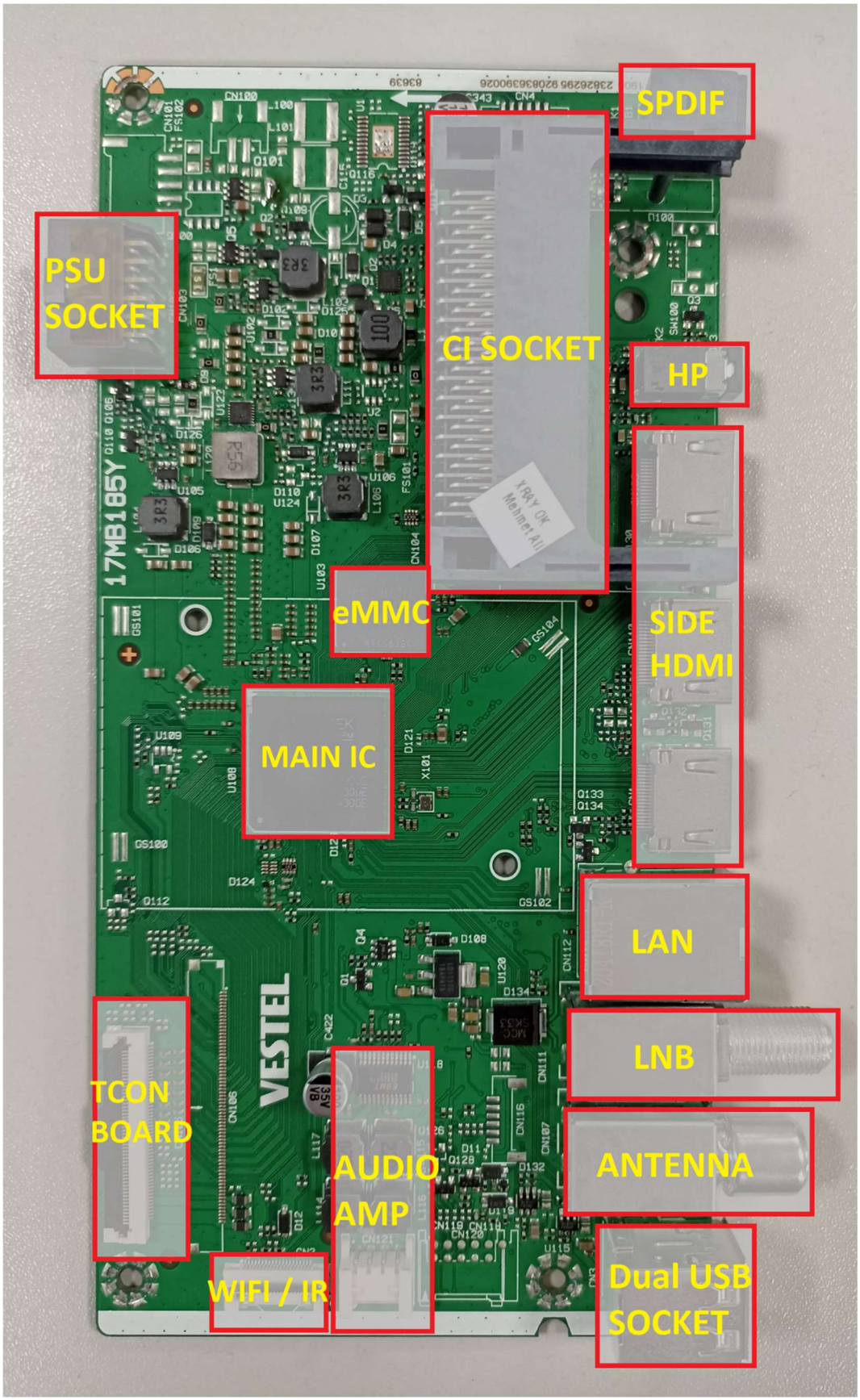
Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF
- 1 Satellite input
- 1 Sub-woofer sound socket
- 3x HDMI inputs (3x side) (with ARC option from 2nd input)
- 1 Common interface(Common)
- 1 Optic/ Quax S/PDIF output
- 1 Headphone(Common)
- 2x USB(1X Side Common, 1X Side Optional) and 1x internal USB for Wifi/Bluetooth
- 1 Ethernet-RJ45
- 1 External Keypad/Tact Switch

A. ***GENERAL BLOCK DIAGRAM***



B. SSB LAYOUT


SPDIF
PSU SOCKET
CI SOCKET
HP
SIDE HDMI
eMMC
MAIN IC
LAN
LNB
TCON BOARD
AUDIO AMP
ANTENNA
WIFI / IR
Dual USB SOCKET
17MB185Y
VESTEL

2. T/T2/C/A TUNER (U107)

Description:

The Si2151 is Silicon Labs' sixth-generation hybrid TV tuner supporting all worldwide terrestrial and cable TV standards. Requiring no external balun, SAW filters, wire wound inductors or LNAs, the Si2151 offers the lowest-cost BOM for a hybrid TV tuner. Also included are an integrated power-on reset circuit and an option for single power supply operation. As with prior-generation Silicon Labs TV tuners, the Si2151 maintains very high linearity and low noise to deliver superior picture quality and a higher number of received stations when compared to other silicon tuners. The Si2151 offers increased immunity to Wi-Fi and LTE interference, eliminating the need for external filtering. For the best performance with next-generation digital TV standards, such as DVB-T2/C2, the Si2151 delivers industry-leading phase noise performance.

Features:

- Worldwide hybrid TV tuner
  - Analog TV: NTSC, PAL/SECAM
  - Digital TV: ATSC/QAM, DVBT2/T/C2/C, ISDB-T/C, DTMB
- 1.7 MHz, 6 MHz, 7 MHz, 8 MHz, and 10 MHz channel bandwidths
- 42-1002 MHz frequency range
- Industry-leading margin to A/74, NorDig, DTG, ARIB, EN55020, OpenCable™, DTMB
- Lowest BOM for a hybrid TV tuner
  - No balun, SAW filters, or external inductors required
  - Increased ESD protection on 4pins
- Best-in-class real-world reception
  - Lowest phase noise
  - High Wi-Fi and LTE immunity
- Low power consumption
  - 3.3 V and 1.8 V power supplies
  - Integrated 1.8 V LDO for 3.3 V single supply operation
- Integrated power-on reset circuit
- Standard CMOS process
- 3x3 mm, 24-pin QFN package
- RoHS compliant

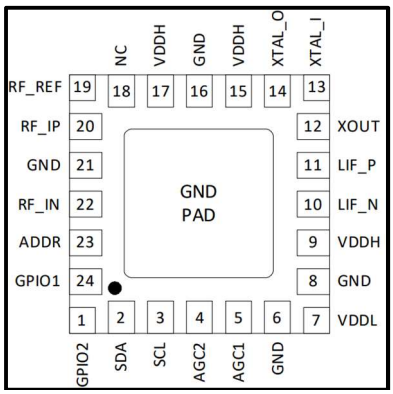


Figure 1: 1 Si2151 Pin description

Pin Number(s)	Name	I/O	Description
1*	GPIO2	I/O	General purpose input/output #1
2	SDA	I/O	I^2C data input/output
3	SCL	I	I^2C clock input
4*	AGC2	I	LIF output amplitude control input #2
5*	AGC1	I	LIF output amplitude control input #1
6	GND	S	Ground
7	VDDL	S	Low supply voltage, 1.8 V (leave caps connected for single supply case)
8	GND	S	Ground
9	VDDH	S	High supply voltage, 3.3 V
10	LIF_N	O	Negative LIF differential output to SoC or DTV/ATV demodulator
11*	LIF_P	O	Positive LIF differential output to SoC or DTV/ATV demodulator
12	XOUT	O	Output reference clock to secondary tuner or receiver
13	XTAL_I	I	Crystal pin 1 (or RCLK input driven by XOUT of another tuner or receiver)
14	XTAL_O	O	Crystal pin 2 (leave floating if XTAL_I is driven by XOUT of another tuner or receiver)
15	VDDH	S	High supply voltage, 3.3 V
16	GND	S	Ground
17	VDDH	S	High supply voltage, 3.3 V
18*	NC	NC	No connect
19	RF_REF	O	RF reference voltage output
20	RF_IP	I	RF input (positive)
21	GND	S	Ground
22	RF_IN	I	RF input (negative)
23	ADDR	I	I^2C address select
24*	GPIO1	I/O	General purpose input/output #1
***Note:** Pin should be left floating if unused.			

3. S/S2 TUNER (U114) OPTIONAL

Description:

M88TS6011 is a single-chip, direct-conversion tuner for digital satellite receiver applications. It offers the industry's most integrated solution to a satellite tuner function, simplifying the front-end designs.

This device incorporates the following functional blocks on a single chip: an LNA, quadrature down-converting mixers, a low phase noise and fast locking frequency synthesizer with on-chip loop filters, a DC offset cancellation loop with integrated loop filters, self-calibrated programmable baseband channel filters, an integrated RF AGC loop, and crystal oscillators with an integrated auxiliary clock output.

As a result of integrating all these blocks, the M88TS6011 has the least number of pins compared with other conventional solutions, and requires the least external components. In typical applications, the M88TS6011 requires only one crystal, one matching network, and a few external capacitors. The device also has the industry's smallest latency, as it uses a fast locking PLL and a fast settling DC offset cancellation architecture.

The M88TS6011 can be configured via a 2-wire serial bus. The chip is available in a 16-pin QFN package.

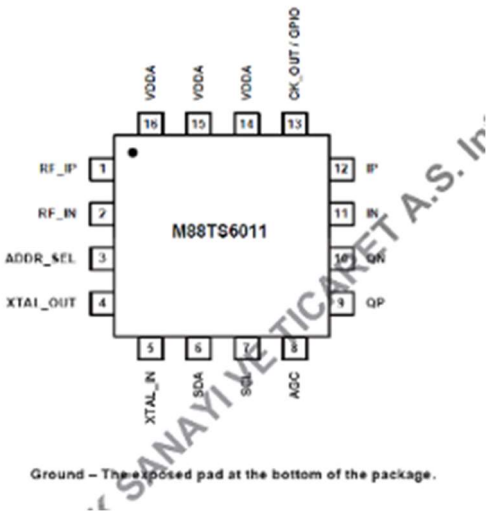
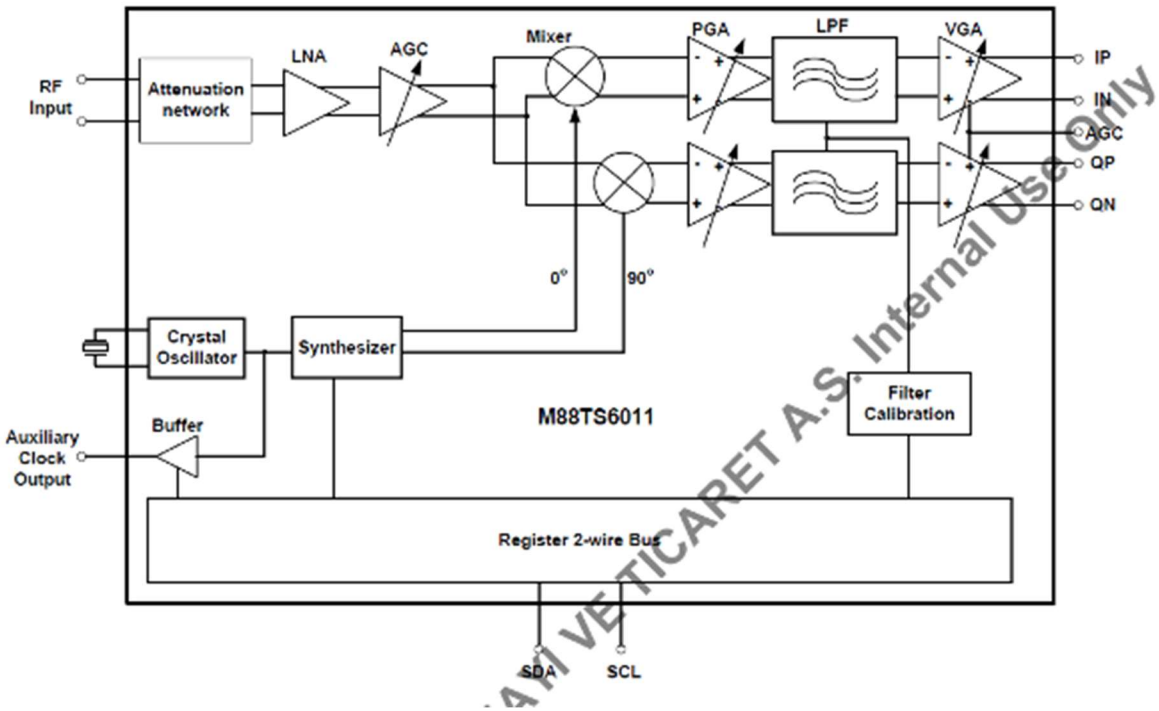


Figure 2: Pin description

Features:

- Single-chip tuner
- Compliant with DVB-S/S2 and ABS-S standards
- Support QPSK, 8PSK, 16APSK and 32APSK
- Direct-conversion from L-band to baseband
- Symbol rate: 1 to 45 Msymbol/s
- Integrated VCOs and PLL, with on-chip inductors, varactors and loop filter
- Integrated baseband filters: 6 MHz to 40 MHz bandwidth
- Integrated RF AGC for optimal performance
- Integrated baseband DC offset cancellation removes external loop filters
- Excellent immunity to strong adjacent undesired channels
- Integrated clock driver provides auxiliary clock output for other devices
- Support sleep mode
- 2-wire serial bus with 3.3 V compatible logic levels
- Power supply: +3.3 V
- Package:16-pin E-PAD QFN
- RoHS compliant

Block Diagram:



4. AUDIO AMPLIFIERS STAGES

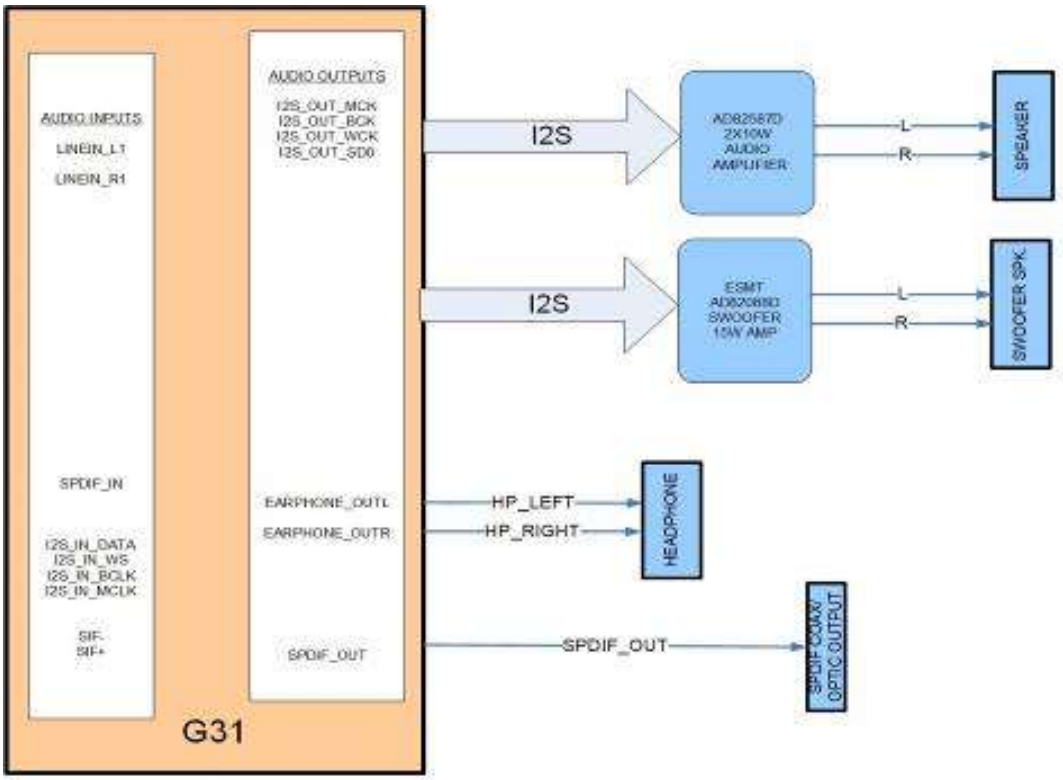


Figure 3: The block diagram of the audio part

A. MAIN AMPLIFIER (U118) (8W/10W/12W OPTIONS)

Description:

AD82587D is a digital audio amplifier capable of driving a pair of 8 ohm, 20W or a single 4 ohm, 40W speaker, both which operate with play music at a 24V supply without external heat-sink or fan requirement.

Using I^2C digital control interface, the user can control AD82587D's input format selection, DRC (dynamic range control), mute and volume control functions. AD82587D has many built-in protection circuits to safeguard AD82587D from connection errors.

Features:

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting) Loudspeaker: 97dB (PSNR), 105dB (DR) @ 24V

- Multiple sampling frequencies (Fs)
  - 32kHz / 44.1kHz / 48kHz and
  - 64kHz / 88.2kHz / 96kHz and
  - 128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x,1024x Fs
  - 256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  - 128x~512x Fs for 64kHz / 88.2kHz / 96kHz
  - 64x~256x Fs for 128kHz /176.4kHz/192kHz
- Supply voltage
  - 3.3V for digital circuit
  - 10V~26V for loudspeaker driver
- Loudspeaker output power for Stereo@ 24V
  - 10W x 2ch into 8_ @ 0.16% THD+N
  - 15W x 2ch into 8_ @ 0.18% THD+N
  - 20W x 2ch into 8_ @ 0.24% THD+N
- Loudspeaker output power for Mono@ 24V
  - 20W x 1ch into 4_ @ 0.17% THD+N
  - 30W x 1ch into 4_ @ 0.2% THD+N
  - 40W x 1ch into 4_ @ 0.24% THD+N
- Sounds processing including:
  - Volume control (+24dB~-103dB, 0.125dB/step)
  - Dynamic range control
  - Power clipping
  - Channel mixing
  - User programmed noise gate with hysteresis window
  - DC-blocking high-pass filter

- Anti-pop design
- Short circuit and over-temperature protection
- I2C control interface with selectable device address
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage
- detection
- Power saving mode
- Dynamic temperature control

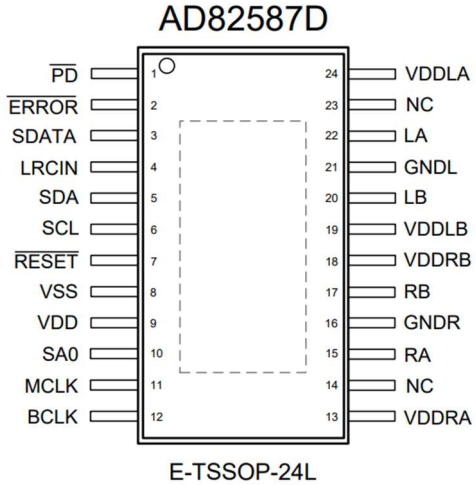


Figure 4: Pin description

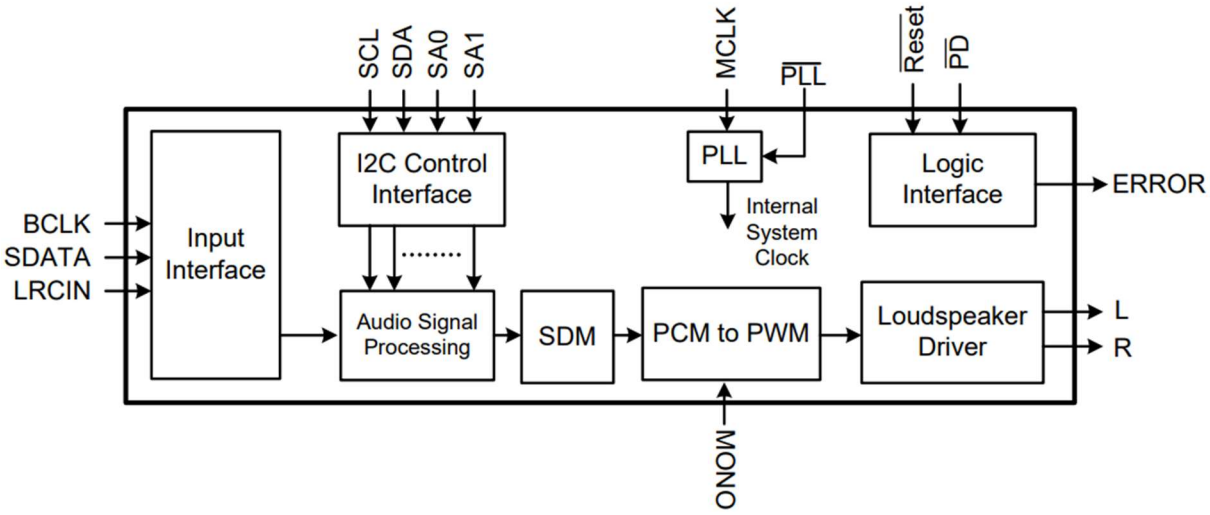


Figure 5: Functional Block Diagram

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

Figure 6: Absolute Maximum Ratings

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~26	V
T_J	Junction Operating Temperature	0~125	°C
T_A	Ambient Operating Temperature	0~70	°C

Figure 7: Recommended Operating Conditions

B. SUBWOOFER AMPLIFIER (U1)

ESMT **AD82088**

2x20W Stereo / 1x40W Mono Digital Audio Amplifier With 30 bands EQ and DRC Functions

Features

- Supply voltage
  3.3V for digital circuit
  8V~26V for loudspeaker driver
- Supports 2.0CH/Mono configuration
- Loudspeaker output power@12V for stereo
  7W x 2CH into 8Ω <1% THD+N
  10W x 2CH into 4Ω <1% THD+N
- Loudspeaker output power@18V for stereo
  15W x 2CH into 8Ω <1% THD+N
- Loudspeaker output power@24V for stereo
  20W x 2CH into 8Ω <1% THD+N
- 16/18/20/24-bits input with I^2S, Left-alignment and Right-alignment data format
- Multiple sampling frequencies (Fs)
  32kHz / 44.1kHz / 48kHz and
  64kHz / 88.2kHz / 96kHz and
  128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  MCLK system:
  64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  64x~512x Fs for 64kHz / 88.2kHz / 96kHz
  64x~256x Fs for 128kHz / 176.4kHz / 192kHz
  BCLK system:
  64xFs for 32kHz / 44.1kHz / 48kHz
  64xFs for 64kHz / 88.2kHz / 96kHz
  64xFs for 128kHz / 176.4kHz / 192kHz
- Sound processing including：
  30 bands parametric speaker EQ
  Volume control (+24dB~-103dB, 0.125dB/step)
  Dynamic range control
  Three Band plus post Dynamic range control
  Power Clipping
  Programmed 3D surround sound
  Channel mixing
  Noise gate with hysteresis window
  Bass/Treble tone control
  DC-blocking high-pass filter
  Pre-scale/post-scale
- Supports I^2C control without clock
- I^2C control interface with selectable device address
- I^2S output with selectable Audio DSP point
- Support hardware and software reset
- Internal PLL
- Anti-pop design
- Level meter and power meter
- LV Under-voltage shutdown and HV Under-voltage detection
- Over voltage protection
- Short circuit and over-temperature protection

Applications

- TV audio

Description

AD82088 is a digital audio amplifier capable of driving 20W (BTL) each to a pair of 8Ω load speaker and 40W (PBTL) to a 4Ω load speaker operating at 24V supply without external heat-sink or fan requirement with play music. AD82088 provides advanced audio processing functions, such as volume control, 30 EQ bands, audio mixing, 3D surround sound and Dynamic Range Control (DRC). These are fully programmable via a simple I^2C control interface. Robust protection circuits are provided to protect AD82088 from damage due to accidental erroneous operating condition. The full digital circuit design of AD82088 is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog class-AB or class-D audio amplifier counterpart implemented by analog circuit design. AD82088 is pop free during instantaneous power on/off or mute/shut down switching because of its robust built-in anti-pop circuit.

Pin Assignment:

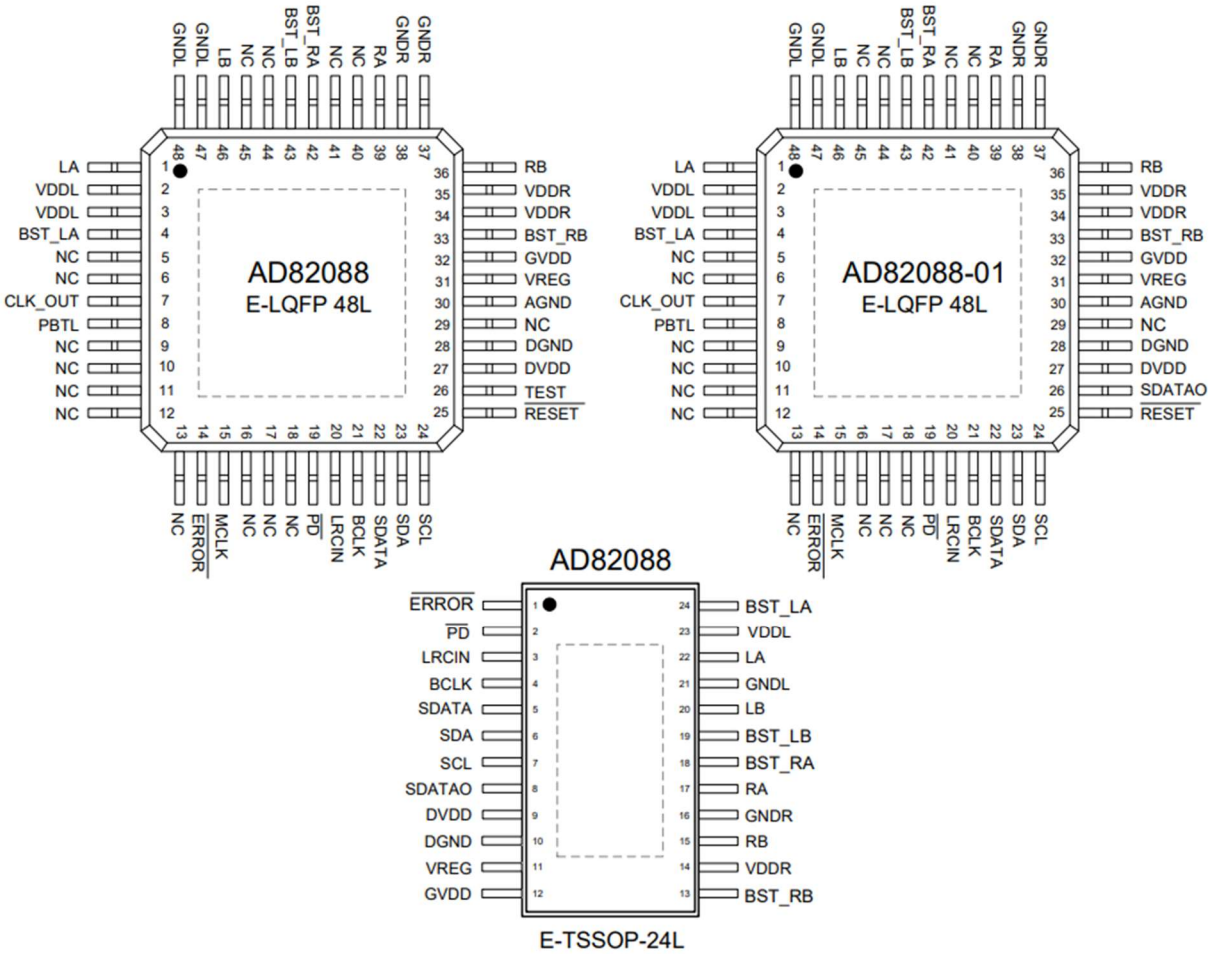


Figure 8: Pin Assignment

Functional Block Diagram:

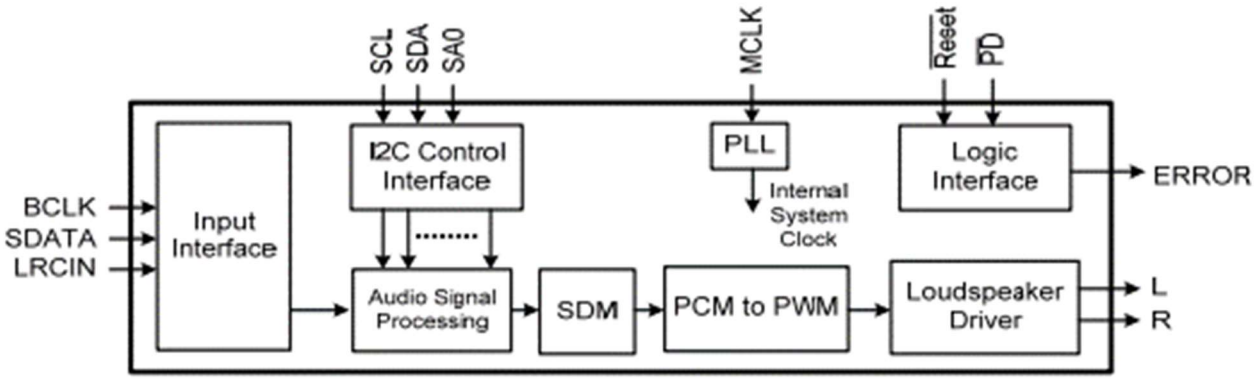


Figure 9: Functional Block Diagram

Pin Description:

PIN	NAME	TYPE	DESCRIPTION	CHARACTERISTICS
1	$\overline{\text{ERROR}}$	I/O	$\overline{\text{ERROR}}$ pin is a dual function pin. One is I^2C address setting during power up. The other one is error status report (low active), It sets by register of A_SEL_FAULT at address 0x1C B[6] to enable it.	This pin is monitored on the rising edge of reset. A value of Low (15-kΩ pull down) sets the I^2C device address to 0x30 and a value of High (15-kΩ pull up) sets it to 0x31.
2	$\overline{\text{PD}}$	I	Power down, low active.	Schmitt trigger TTL input buffer, internal pull High with a 330Kohm resistor.
3	LRCIN	I	Left/Right clock input (Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
4	BCLK	I	Bit clock input (64Fs).	Schmitt trigger TTL input buffer, internal pull Low with a 100Kohm resistor.
5	SDATA	I	Serial audio data input.	Schmitt trigger TTL input buffer
6	SDA	I/O	I^2C bi-directional serial data.	Schmitt trigger TTL input buffer
7	SCL	I	I^2C serial clock input.	Schmitt trigger TTL input buffer
8	SDATAO	O	Serial audio data output.	Schmitt trigger TTL input buffer
9	DVDD	P	Digital Power.	
10	DGND	P	Digital Ground.	
11	VREG	O	1.8V Regulator voltage output.	
12	GVDD	O	5V Regulator voltage output. This pin must not be used to drive external devices.	
13	BST_RB	P	Bootstrap supply for right channel output B.	
14	VDDR	P	Right channel supply.	
15	RB	O	Right channel output B.	
16	GNDR	P	Right channel ground.	
17	RA	O	Right channel output A.	
18	BST_RA	P	Bootstrap supply for right channel output A.	
19	BST_LB	P	Bootstrap supply for left channel output B.	
20	LB	O	Left channel output B.	
21	GNDL	P	Left channel ground.	
22	LA	O	Left channel output A.	
23	VDDL	P	Left channel supply.	
24	BST_LA	P	Bootstrap supply for left channel output A.	

Figure 10: Pin Description

5. POWER STAGE

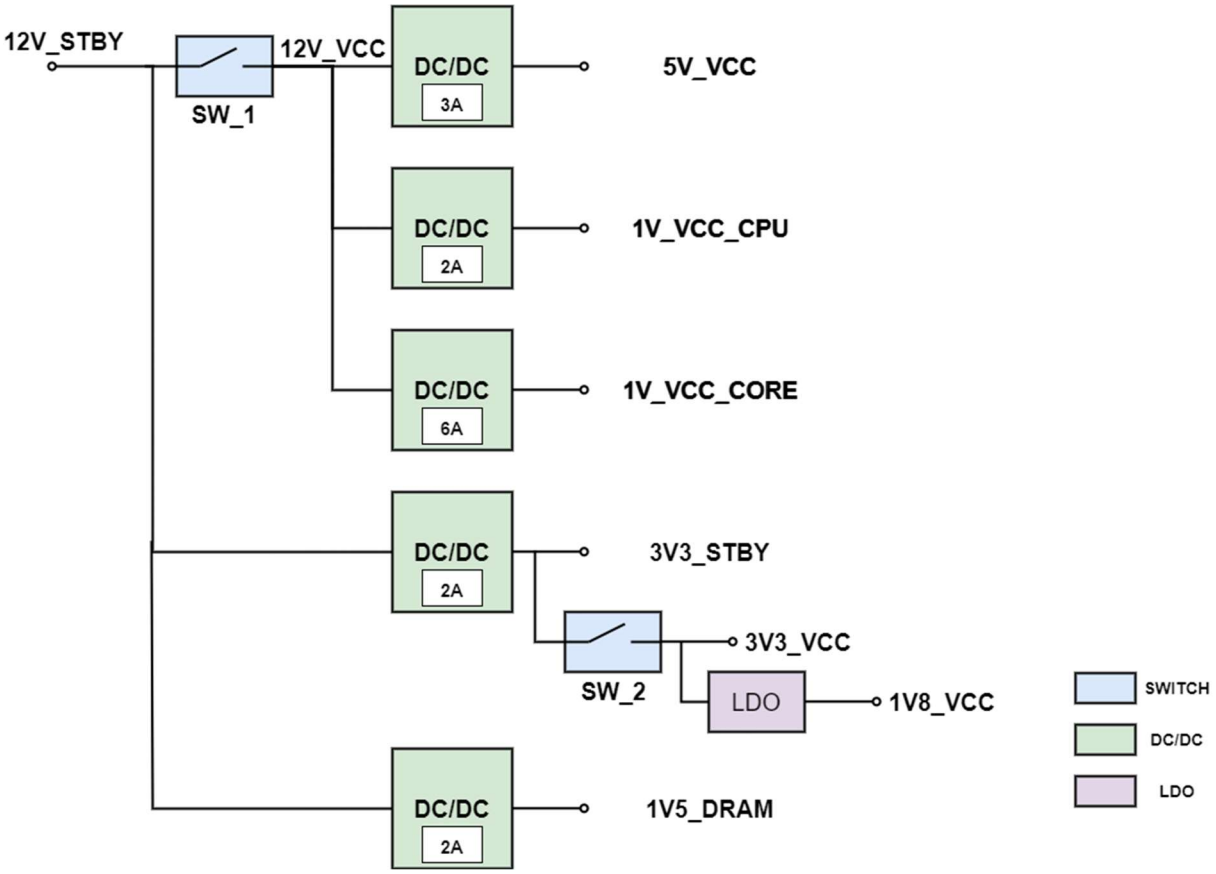


Figure 11: Power Block Diagram

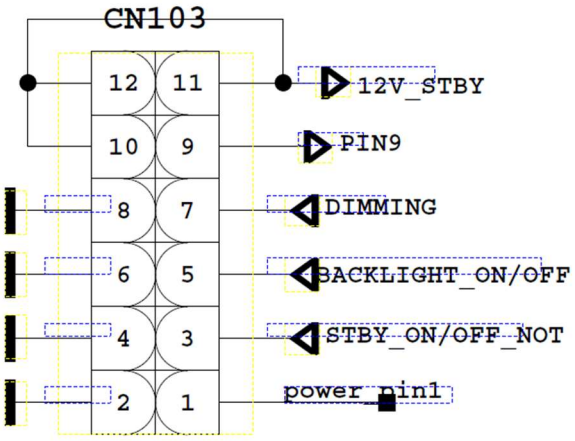


Figure 12: Socket and Power Options

Power socket is used for taking 12V_STBY voltage which is produced in power card. Also socket is used for giving dimming, backlight and standby signals with power card. Power socket pinning is shown in above figure.

12V_STBY is converted several different voltages on the mainboard which are shown in below figure.

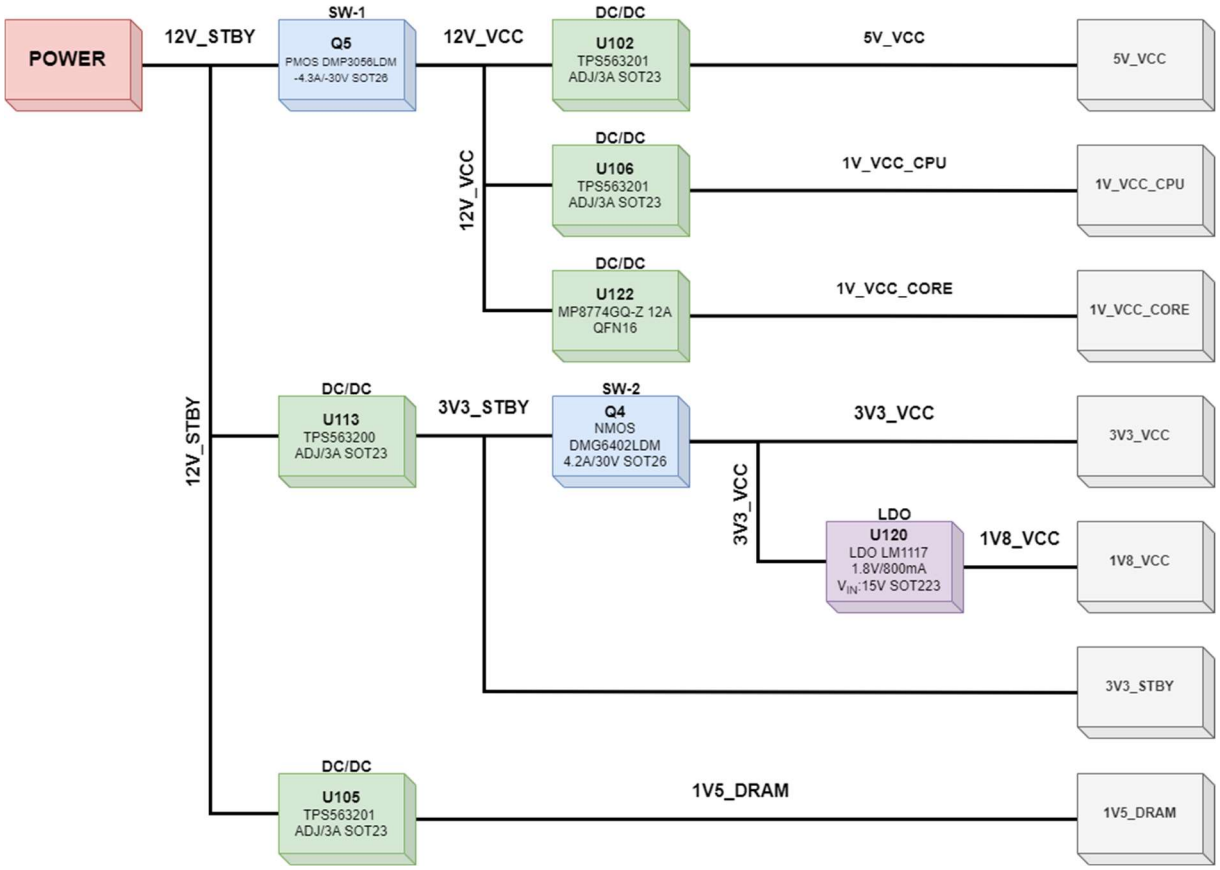


Figure 13: Power Block Diagram

List of the components:

- SW-1 (Q5) → PMOS DMP3056LDM -4.3A/-30V
- SW-2 (Q4) → NMOS DMG6402LDM 4.2A/30V
- DC-DC-1 (U102) → TPS563201 ADJ/3A
- DC-DC-2 (U105) → TPS563201 ADJ/3A
- DC-DC-3 (U106) → TPS563201 ADJ/3A
- DC-DC-4 (U113) → TPS563200 ADJ/3A
- DC-DC-5 (U122) → MP8774GQ-Z 12A
- LDO-1 (U120) → LM1117 1.8V/800Ma 15V

A. ***DMP3056LDM -4.3A/-30V (Q5)***

DIODES INCORPORATED

Lead-free Green

DMP3056LDM

P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)\ max}$	I_D $T_A = 25°C$
-30V	45mΩ @ V_{GS} = -10V	-4.3A
	65mΩ @ V_{GS} = -4.5V	-3.3A

Description

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

- General Purpose Interfacing Switch
- Power Management Functions
- Analog Switch

Features

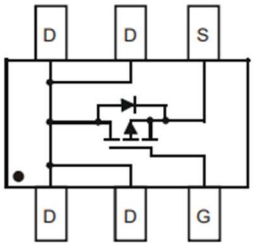
- Low Gate Threshold Voltage
- Low On-Resistance
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

- Case: SOT26
- Case Material – Molded Plastic, "Green" Molding Compound. UL Flammability Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208
- Terminal Connections: See Diagram
- Weight: 0.008 grams (approximate)

SOT26

Top View



Top View
Internal Schematic

Figure 14: Pin Description

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
STATIC PARAMETERS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	V_{GS} = 0V, I_D = -250μA
Zero Gate Voltage Drain Current T_J = +25°C	I_{DSS}	—	—	-1	μA	V_{GS} = 0V, V_{DS} = -30V
Gate-Body Leakage Current	I_{GSS}	—	—	±100 ±800	nA	V_{GS} = ±20V, V_{DS} = 0V V_{GS} = ±25V, V_{DS} = 0V
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	—	-2.1	V	V_{GS} = V_{DS}, I_D = -250μA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	—	— —	45 65	mΩ	V_{GS} = -10V, I_D = -5A V_{GS} = -4.5V, I_D = -4.2A
Forward Transconductance	g_{FS}	—	8	—	S	V_{DS} = -10V, I_D = -4.3A
Diode Forward Voltage	V_{SD}	—	—	-1.2	V	V_{GS} = 0V, I_S = -1.7A
DYNAMIC PARAMETERS (Note 8)						
Input Capacitance	C_{iss}	—	948	—	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0MHz
Output Capacitance	C_{oss}	—	105	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	100	—	pF	
SWITCHING CHARACTERISTICS (Note 8)						
Total Gate Charge	Q_G	—	10.1	—	nC	V_{DS} = -15V, V_{GS} = -4.5V, I_D = -6A
	Q_G	—	21.1	—	nC	V_{DS} = -15V, V_{GS} = -10V, I_D = -6A
Gate-Source Charge	Q_{GS}	—	2.8	—		
Gate-Drain Charge	Q_{GD}	—	3.2	—		
Gate Resistance	R_g	—	13.15	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Turn-On Delay Time	$t_{d(on)}$	—	10.2	—	ns	V_{DS} = -15V, V_{GS} = -10V, I_D = -1A, R_G = 6.0Ω
Rise Time	t_r	—	6.6	—		
Turn-Off Delay Time	$t_{d(off)}$	—	50.1	—		
Fall Time	t_f	—	22.3	—		

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	-30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 6) V_{GS} = 10V	Steady State	T_A = +25°C	I_D	-4.3	A
	t < 10s	T_A = +25°C	I_D	-5.8	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	-2.3	A
Pulsed Drain Current (10μs pulse, duty cycle = 1%)			I_{DM}	-13	A

Thermal Characteristics

Characteristic		Symbol	Value	Units
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	1.25	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	100	°C/W
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	1.5	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	86	°C/W
Thermal Resistance, Junction to Case		$R_{\theta JC}$	15.6	
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Table 1: Electrical Characteristics & Maximum Ratings & Thermal Characteristics

B. DMG6402LDM 4.2A/30V (Q4)

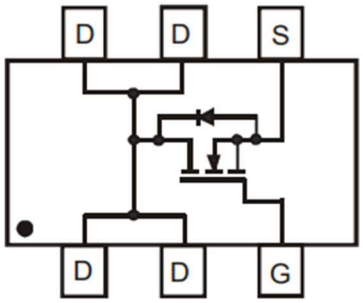
Features:

- Low RDS(ON)
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage

- Lead Free By Design/RoHS Compliant (Note 1)
- Qualified to AEC-Q101 Standards for High Reliability
- "Green" Device (Note 2)

SOT-26

TOP VIEW



TOP VIEW
Internal Schematic

Figure 15: Pin Description

Electrical Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 5)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current T_J = 25°C	I_{DSS}	-	-	1.0	μA	V_{DS} = 30V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	-	-	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 5)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	1.5	2.0	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	-	22 32	27 40	mΩ	V_{GS} = 10V, I_D = 7A V_{GS} = 4.5V, I_D = 5.6A
Forward Transfer Admittance	$\|Y_{fs}\|$	-	10	-	S	V_{DS} = 5V, I_D = 7A
Diode Forward Voltage	V_{SD}	-	0.75	1.0	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 6)						
Input Capacitance	C_{iss}	-	404	-	pF	V_{DS} =15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	-	52	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	45	-	pF	
Gate Resistance	R_g	-	1.51	-	Ω	V_{DS} =0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	-	9.2	-	nC	V_{GS} =10V, V_{DS} = 15V, ID =5.8A
Gate-Source Charge	Q_{gs}	-	1.2	-	nC	
Gate-Drain Charge	Q_{gd}	-	1.8	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	3.41	-	ns	V_{DD} = 15V, V_{GS} = 10V, R_L = 2.6Ω, R_G = 3Ω
Turn-On Rise Time	t_r	-	6.18	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	13.92	-	ns	
Turn-Off Fall Time	t_f	-	2.84	-	ns	

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 3)	P_D	1.12	W
Thermal Resistance, Junction to Ambient T_A = 25°C (Note 3)	$R_{\theta JA}$	111	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Maximum Ratings @T_A = 25°C unless otherwise specified

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current (Note 3)	Steady State	T_A = 25°C T_A = 70°C	I_D	5.3 4.2	A
Pulsed Drain Current (Note 4)			I_{DM}	31	A

Table 2: Electrical Characteristics & Thermal Characteristics & Maximum Ratings

C. TPS563201 (U102, U105, U106)

General Description:

The TPS563201 is simple, easy-to-use, 3 A synchronous step-down converter in SOT-23 package. The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current. These switch mode power supply (SMPS) devices employ D-CAP2 mode control providing a fast transient response and supporting both low-equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components. TPS563201 operates in pulse skip mode, which maintains high efficiency during light load operation. The TPS563201 is available in a 6-pin 1.6-mm x 2.9-mm SOT (DDC) package, and specified from a -40°C to 125°C junction temperature.

Features:

- TPS563201 and TPS563208 3-A Converter Integrated 95-m0 and 57-m0 FETs
- D-CAP2TM Mode Control with fast transient response
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- Pulse-skip mode
- 580-kHz Switching Frequency
- Low Shutdown Current Less than 10 pA
- 2% Feedback Voltage Accuracy (25 °C)
- Startup from Pre-Biased Output Voltage
- Cycle-by-Cycle Overcurrent Limit • Hiccup-mode Overcurrent Protection
- Non-Latch UVP and TSD Protections
- Fixed Soft Start: 1.0 ms

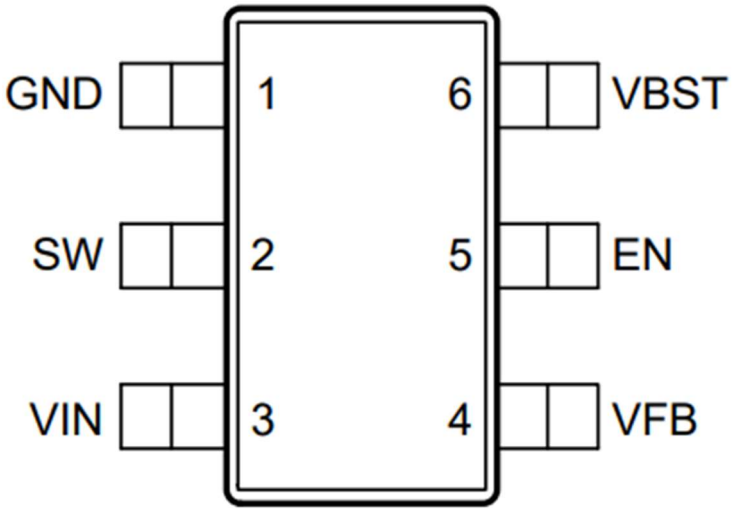


Figure 16: Pin Description

Functional Pin Descriptions:

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
VIN	3	I	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	I	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 µF capacitor between VBST and SW pins.

Table 3: Functional Pin Description

Electrical Characteristics:

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{VIN}	Operating – non-switching supply current	V_{IN} current, EN = 5 V, V_{FB} = 0.8 V	TPS563201		380	520	µA
			TPS563208		590	750	
I_{VINSDN}	Shutdown supply current	V_{IN} current, EN = 0 V			1	10	µA
LOGIC THRESHOLD							
V_{ENH}	EN high-level input voltage	EN		1.6			V
V_{ENL}	EN low-level input voltage	EN				0.8	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V		225	400	900	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE							
V_{FBTH}	V_{FB} threshold voltage	V_O = 1.05 V, I_O = 10 mA, Eco-mode™ operation			774		mV
	V_{FB} threshold voltage	V_O = 1.05 V, continuous mode operation		749	768	787	mV
I_{VFB}	V_{FB} input current	V_{FB} = 0.8 V			0	±0.1	µA
MOSFET							
$R_{DS(on)h}$	High-side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V			95		mΩ
$R_{DS(on)l}$	Low-side switch resistance	T_A = 25°C			57		mΩ
CURRENT LIMIT							
I_{ocl}	Current limit	DC current, V_{OUT} = 1.05 V, L_1 = 1.5 µH		3.3	4.2	5.1	A
THERMAL SHUTDOWN							
T_{SDN}	Thermal shutdown threshold(1)	Shutdown temperature			172		°C
		Hysteresis			37		
ON-TIME TIMER CONTROL							
$t_{OFF(MIN)}$	Minimum off time	V_{FB} = 0.5 V			220	310	ns
SOFT START							
Tss	Soft-start time	Internal soft-start time			1.0		ms
FREQUENCY							
F_{sw}	Switching frequency	V_{IN} = 12 V, V_O = 1.05 V, FCCM mode			580		kHz
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION							
V_{UVP}	Output UVP threshold	Hiccup detect (H > L)			65%		
T_{HICCUP_WAIT}	Hiccup on time				1.8		ms
T_{HICCUP_RE}	Hiccup time before restart				15		ms
UVLO							
UVLO	UVLO threshold	Wake up VIN voltage			4.0	4.3	V
		Shutdown VIN voltage		3.3	3.6		
		Hysteresis VIN voltage			0.4		

Recommended Operating Conditions:

			MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage range		4.5		17	V
V_I	Input voltage range	VBST	–0.1		23	V
		VBST (10 ns transient)	–0.1		26	
		VBST (vs SW)	–0.1		6.0	
		EN	–0.1		17	
		VFB	–0.1		5.5	
		SW	–1.8		17	
		SW (10 ns transient)	–3.5		20	
T_J	Operating junction temperature		–40		125	°C

Maximum Ratings:

		MIN	MAX	UNIT
Input voltage	VIN, EN	–0.3	19	V
	VBST	–0.3	25	V
	VBST (10 ns transient)	–0.3	27	V
	VBST (vs SW)	–0.3	6.5	V
	VFB	–0.3	6.5	V
	SW	–2	19	V
	SW (10 ns transient)	–3.5	21	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

Table 4: Electrical Characteristics & Recommended Operating Conditions & Maximum Ratings

D. TPS563200 (U113)

General Description:

The TPS562200 and TPS563200 are simple, easy-to-use, 2 A and 3 A synchronous step-down (buck) converters in 6 pin SOT-23 package. The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current. These switch mode power supply (SMPS) devices employ D-CAP2 mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components. TPS562200 and TPS563200 operate in Advanced Eco-mode, which maintains high efficiency during light load operation. The devices are available in a 6-pin 1.6mm x 2.9mm SOT (DDC) package, and specified from -40°C to 85°C of ambient temperature.

Features:

- TPS562200 - 2A converter with Integrated 122 mΩ and 72 mΩ FETs
- TPS563200 - 3A converter with Integrated 68 mΩ and 39 mΩ FETs
- D-CAP2™ Mode Control for Fast Transient Response
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- 650 kHz Switching Frequency
- Advanced Eco-mode™ Pulse-skip
- Low Shutdown Current Less than 10 µA
- 1% Feedback Voltage Accuracy (25°C)
- Startup from Pre-Biased Output Voltage
- Cycle-By-Cycle Overcurrent Limit
- Hiccup-Mode Undervoltage Protection
- Non-latch OVP, UVLO and TSD Protections
- Fixed Soft Start: 1 ms

Applications:

- Digital TV Power Supply
- High Definition Blu-ray Disc™ Players
- Networking Home Terminal
- Digital Set Top Box (STB)

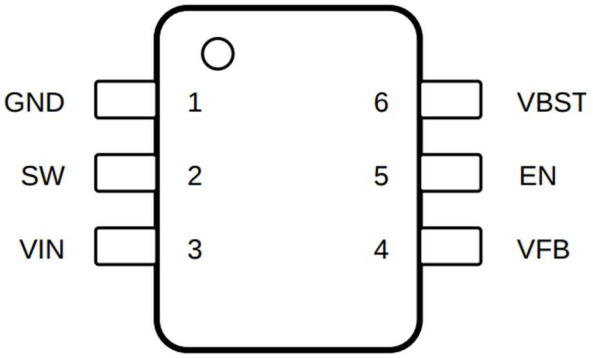


Figure 17: Pin Description

Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
GND	1	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET.
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	Supply input for the high-side NFET gate drive circuit. Connect a 0.1µF capacitor between VBST and SW pins.

Absolute Maximum Ratings:

		MIN	MAX	UNIT
Input voltage range	VIN, EN	–0.3	19	V
	VBST	–0.3	25	V
	VBST (10 ns transient)	–0.3	27.5	V
	VBST (vs SW)	–0.3	6.5	V
	VFB	–0.3	6.5	V
	SW	–2	19	V
	SW (10 ns transient)	–3.5	21	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature range, T_{stg}		–55	150	°C

Table 5: Pin Functions & Absolute Maximum Ratings

Recommended Operating Conditions:

			MIN	MAX	UNIT
V_{IN}	Supply input voltage range		4.5	17	V
V_I	Input voltage range	VBST	–0.1	23	V
		VBST (10 ns transient)	–0.1	26	
		VBST(vs SW)	–0.1	6	
		EN	–0.1	17	
		VFB	–0.1	5.5	
		SW	–1.8	17	
		SW (10 ns transient)	–3.5	20	
T_A	Operating free-air temperature		–40	85	°C

Electrical Characteristics:

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
$I_{(VIN)}$	Operating – non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5V, V_{FB} = 0.8 V	TPS562200		230	330	µA
			TPS563200		190	290	
$I_{(VINSDN)}$	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V			3	10	µA
LOGIC THRESHOLD							
$V_{EN(H)}$	EN high-level input voltage	EN		1.6			V
$V_{EN(L)}$	EN low-level input voltage	EN				0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V		225	450	900	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE							
$V_{FB(TH)}$	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V, I_O = 10mA, Eco-mode™ operation			772		mV
		T_A = 25°C, V_O = 1.05 V, continuous mode operation		758	765	772	mV
$I_{(VFB)}$	V_{FB} input current	V_{FB} = 0.8V, T_A = 25°C			0	±0.1	µA
MOSFET							
$R_{DS(on)h}$	High side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V	TPS562200		122		mΩ
			TPS563200		68		mΩ
$R_{DS(on)l}$	Low side switch resistance	T_A = 25°C	TPS562200		72		mΩ
			TPS563200		39		mΩ
CURRENT LIMIT							
I_{ocl}	Current limit (1)	DC current, V_{OUT} = 1.05 V, L_{OUT} = 2.2 µF	TPS562200	2.5	3.2	4.3	A
		DC current, V_{OUT} = 1.05 V, L_{OUT} = 1.5 µF	TPS563200	3.5	4.2	5.3	A
THERMAL SHUTDOWN							
T_{SDN}	Thermal shutdown threshold (1)	Shutdown temperature			155		°C
		Hysteresis			35		
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION							
V_{OVP}	Output OVP threshold	OVP Detect			125% x Vfbth		
V_{UVP}	Output Hiccup threshold	Hiccup detect			65% x Vfbth		
$t_{HiccupOn}$	Hiccup On Time	Relative to soft-start time			1		ms
$t_{HiccupOff}$	Hiccup Off Time	Relative to soft-start time			7		ms
UVLO							
UVLO	UVLO threshold	Wake up VIN voltage		3.45	3.75	4.05	V
		Hysteresis VIN voltage		0.13	0.32	0.55	

Table 6: Recommended Operating Conditions & Electrical Characteristics

E. MP8774GQ-Z (U122)

DESCRIPTION

The MP8774 is a fully integrated high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. The MP8874 offers a very compact solution that achieves 12A of continuous output current with excellent load and line regulation over a wide input range. The MP8774 uses synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time (COT) control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP8774 requires a minimal number of readily available, standard, external components and is available in a space-saving QFN-16 (3mmx3mm) package.

FEATURES

- Output Adjustable from 0.6V
- Wide 3V to 18V Operating Input Range
- 12A Output Current
- 16mΩ/5.5mΩ Low $R_{DS(ON)}$ Internal Power MOSFETs
- 100μA Quiescent Current
- High-Efficiency Synchronous Mode Operation
- Pre-Biased Start-Up
- Fixed 700kHz Switching Frequency
- External Programmable Soft Start-Up Time
- Enable (EN) and Power Good (PG) for Power Sequencing
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Available in a QFN-16 (3mmx3mm) Package

APPLICATIONS

- Security Cameras
- Portable Devices, XDSL Devices
- Digital Set-Top Boxes
- Flat-Panel Television and Monitors
- General Purpose

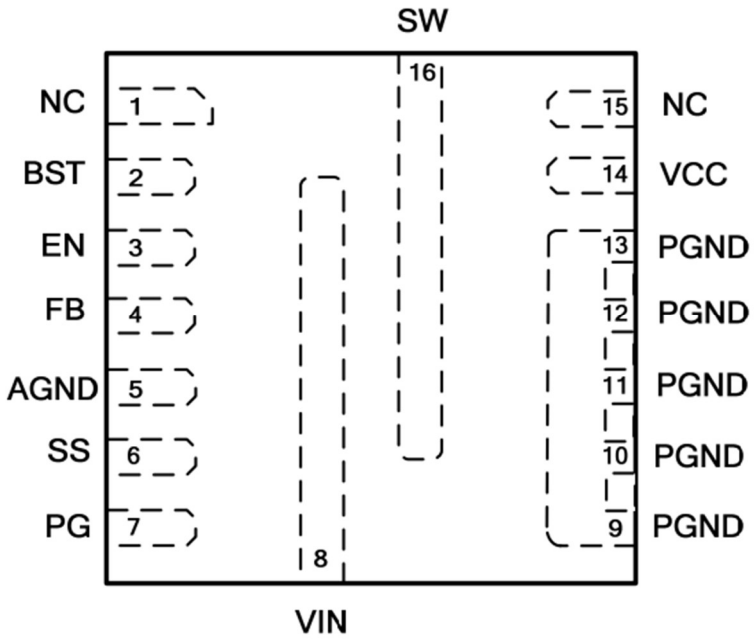
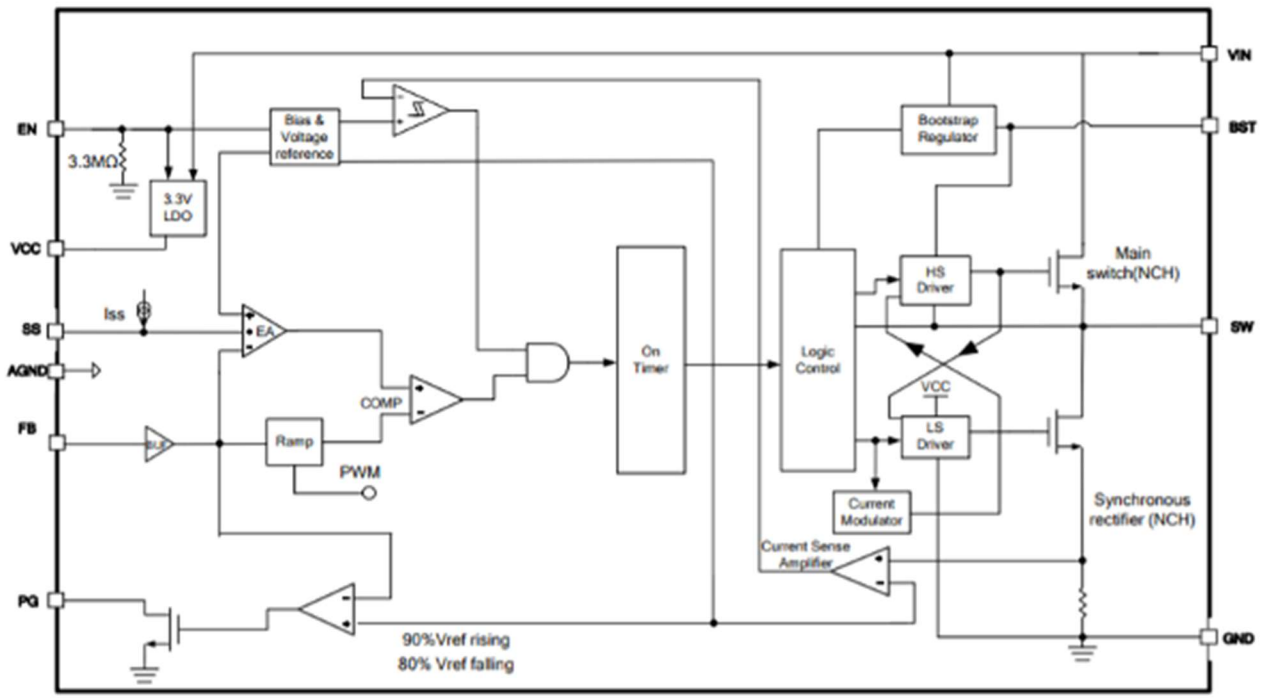


Figure 18: Pin Description

PIN FUNCTIONS

Package Pin #	Name	Description
1, 15	NC	**No connection.** NC must be left floating.
2	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver. A BST resistor less than 4.7Ω is recommended.
3	EN	**Enable.** Pull EN high to enable the MP8774. When floating, EN is pulled down to GND and disabled by an internal 3.3MΩ resistor.
4	FB	**Feedback.** FB sets the output voltage when connected to the tap of an external resistor divider between output and GND.
5	AGND	**Signal ground.** AGND is not connected to the system ground internally. Ensure that AGND is connected to the system ground in the PCB layout.
6	SS	**Soft start.** Connect a capacitor across SS and GND to set the soft-start time to avoid inrush current at start-up.
7	PG	**Power good output.** The output of PG is an open drain. PG changes state if UVP, OCP, OTP, or OV occurs.
8	VIN	**Supply voltage.** The MP8774 operates from a 3 - 18V input rail. A capacitor (C1) is needed to decouple the input rail. Use a wide PCB trace to make the connection.
9 - 13	PGND	**System ground.** PGND is the reference ground of the regulated output voltage. PGND requires careful consideration during the PCB layout. PGND is recommended to be connected to GND with coppers and vias.
14	VCC	**Internal bias supply output.** Decouple VCC with a 1μF capacitor. Place the VCC capacitor close to VCC and GND.
16	SW	**Switch output.** Connect SW with a wide PCB trace.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (6)

V_{IN} = 12V, T_J = -40°C to +125°C, typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input voltage range	V_{IN}		3		18	V
Supply Current						
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			5	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.65V		100	150	μA
MOSFET						
HS switch on resistance	$HS_{RDS(ON)}$	V_{BST-SW} = 3.3V		16		mΩ
LS switch on resistance	$LS_{RDS(ON)}$	V_{CC} = 3.3V		5.5		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 17V, T_J = 25°C			1	μA
Current Limit and ZCD						
Valley current limit	I_{LIMIT_VY}		12	14		A
Short hiccup duty cycle (7)	D_{HICCUP}			10		%
ZCD	I_{ZCD}			200		mA
Switching Frequency and Minimum On/Off Timer						
Switching frequency	Fs		600	700	800	kHz
Minimum on time (7)	$T_{On\ MIN}$			50		ns
Minimum off time (7)	$T_{Off\ MIN}$			100		ns
Reference and Soft Start						
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
		T_J = -40°C to +125°C	591	600	609	
Feedback current	I_{FB}	V_{FB} = 700mV		10	50	nA
Soft-start current	I_{SS_START}		4	6	8	μA
Enable and UVLO						
EN rising threshold	$V_{EN\ RISING}$		1.1	1.25	1.4	V
EN falling threshold	$V_{EN\ FALLING}$		0.9	1	1.1	V
EN pull-down resistor	R_{EN_PD}			1.2		MΩ
VCC						
VCC under-voltage lockout threshold rising	VCC_{Vth}		2.6	2.8	3	V
VCC under-voltage lockout threshold	VCC_{HYS}			350		mV
VCC regulator	V_{CC}			3.4		V
VCC load regulation	Reg_{VCC}	I_{CC} = 5mA		3		%
Power Good						
Power good UV rising threshold	$PGUV_{vth\_Hi}$		0.85	0.9	0.95	V_{FB}
Power good UV falling threshold	$PGUV_{vth\_Lo}$		0.75	0.80	0.85	V_{FB}
Power good OV rising threshold	$PGOV_{vth\_Hi}$		1.15	1.2	1.25	V_{FB}
Power good OV falling threshold	$PGOV_{vth\_Lo}$		1.05	1.1	1.15	V_{FB}
Power good delay	PG_{Td}	Both edge		50		μs
Power good sink current capability	V_{PG}	Sink 4mA			0.4	V
Power good leakage current	I_{PG_LEAK}	V_{PG} = 5V			10	μA
Thermal Protection						
Thermal shutdown (7)	T_{SD}			150		°C
Thermal hysteresis (7)	T_{SD-HYS}			20		°C

Table 7: Electrical Characteristics

Absolute Maximum Ratings:

V_{IN}	-0.3V to +20V
V_{SW}	-0.3V (-5V < 10ns) to V_{IN} + 0.7V (23V < 10ns)
V_{BST}	V_{SW} + 4V
V_{EN}	V_{IN}
All other pins	-0.3V to +4V
Continuous power dissipation (T_A=+25°C)	3.2W
Junction temperature	150°C
Lead temperature	260°C
Storage temperature	-65°C to 125°C

Recommended Operating Conditions:

V_{IN}	3V to 18V
V_{OUT}	0.6V to VIN * DMAX or 12V max
T_J	-40°C to +125°C

Table 8: Absolute Maximum Ratings & Recommended Operating Conditions

F. LM1117 (U120)

Description:

The LM1117 is a low dropout voltage regulator with a dropout of 1.2 V at 800 mA of load current. The LM1117 is available in an adjustable version, which can set the output voltage from 1.25 V to 13.8 V with only two external resistors. In addition, the device is available in five fixed voltages, 1.8 V, 2.5 V, 3.3 V, and 5 V. The LM1117 offers current limiting and thermal shutdown. The circuit includes a Zener trimmed bandgap reference to assure output voltage accuracy to within ±1%. A minimum of 10-µF tantalum capacitor is required at the output to improve the transient response and stability.

Features:

- Available in 1.8 V, 2.5 V, 3.3 V, 5 V, and adjustable versions
- Space-saving SOT-223 and WSON packages
- Current limiting and thermal protection
- Output current: 800 mA
- Line regulation: 0.2% (maximum)
- Load regulation: 0.4% (maximum)
- Temperature range: – LM1117: 0°C to +125°C
- **Pin Description:**

- **Pin Description:**

Pin Description:

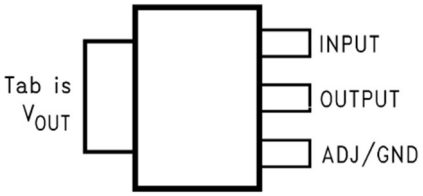


Figure 19: Pin Description

PIN						I/O	DESCRIPTION
NAME	TO-252	WSON	SOT-223	TO-263	TO-220		
ADJ/GND	1	1	1	1	1	—	Adjust pin for adjustable output option. Ground pin for fixed output option.
V_{IN}	3	2, 3, 4	3	3	3	I	Input voltage pin for the regulator
V_{OUT}	2 , TAB	5, 6, 7, TAB	2, 4	2, TAB	2, TAB	O	Output voltage pin for the regulator

Absolute Maximum Ratings:

	MIN	MAX	UNIT
Maximum input voltage (V_{IN} to GND)		20	V
Power dissipation[2]	Internally Limited		
Junction temperature (T_J)[2]		150	°C
Storage temperature, T_{stg}	–65	150	°C

Recommended Operating Conditions:

		MIN	MAX	UNIT
Input voltage (V_{IN} to GND)			15	V
Junction temperature (T_J)[1]	LM1117	0	125	°C
	LM1117I	–40	125	

Table 9: Pin Functions & Absolute Maximum Ratings & Recommended Operating Conditions

Functional Block Diagram:

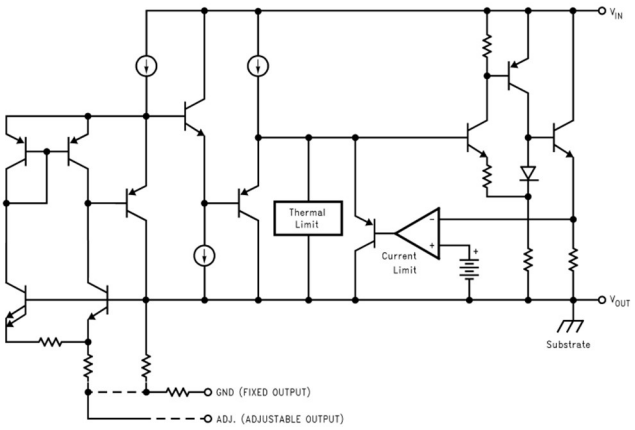


Figure 20: Functional Block Diagram

Electrical Characteristics:

PARAMETER		TEST CONDITIONS		MIN[1]	TYP[2]	MAX[1]	UNIT
V_{REF}	Reference voltage	LM1117-ADJ I_{OUT} = 10 mA, $V_{IN} - V_{OUT}$ = 2 V, T_J = 25°C		1.238	1.25	1.262	V
		LM1117-ADJ 10 mA ≤ I_{OUT} ≤ 800 mA, 1.4 V ≤ $V_{IN} - V_{OUT}$ ≤ 10 V	T_J = 25°C		1.25		
			over the junction temperature range 0°C to 125°C	1.225		1.27	
V_{OUT}	Output voltage	LM1117-1.8 I_{OUT} = 10 mA, V_{IN} = 3.8 V, T_J = 25°C		1.782	1.8	1.818	V
		LM1117-1.8 0 ≤ I_{OUT} ≤ 800 mA, 3.2 V ≤ V_{IN} ≤ 10 V	T_J = 25°C		1.8		
			over the junction temperature range 0°C to 125°C	1.746		1.854	
		LM1117-2.5 I_{OUT} = 10 mA, V_{IN} = 4.5 V, T_J = 25°C		2.475	2.5	2.525	V
		LM1117-2.5 0 ≤ I_{OUT} ≤ 800 mA, 3.9 V ≤ V_{IN} ≤ 10 V	T_J = 25°C		2.5		
			over the junction temperature range 0°C to 125°C	2.45		2.55	
		LM1117-3.3 I_{OUT} = 10 mA, V_{IN} = 5 V T_J = 25°C		3.267	3.3	3.333	V
		LM1117-3.3 0 ≤ I_{OUT} ≤ 800 mA, 4.75 V ≤ V_{IN} ≤ 10 V	T_J = 25°C		3.3		
			over the junction temperature range 0°C to 125°C	3.235		3.365	
		LM1117-5.0 I_{OUT} = 10 mA, V_{IN} = 7 V, T_J = 25°C		4.95	5	5.05	V
		LM1117-5.0 0 ≤ I_{OUT} ≤ 800 mA, 6.5 V ≤ V_{IN} ≤ 12 V	T_J = 25°C		5		
			over the junction temperature range 0°C to 125°C	4.9		5.1	
ΔV_{OUT}	Line regulation[3]	LM1117-ADJ I_{OUT} = 10mA, 1.5V ≤ V_{IN}-V_{OUT} ≤ 13.75V	T_J = 25°C		0.035%		
			over the junction temperature range 0°C to 125°C			0.2%	
		LM1117-1.8 I_{OUT} = 0 mA, 3.2 V ≤ V_{IN} ≤ 10 V	T_J = 25°C		1		mV
			over the junction temperature range 0°C to 125°C			6	
		LM1117-2.5 I_{OUT} = 0 mA, 3.9 V ≤ V_{IN} ≤ 10 V	T_J = 25°C		1		mV
			over the junction temperature range 0°C to 125°C			6	
		LM1117-3.3 I_{OUT} = 0 mA, 4.75 V ≤ V_{IN} ≤ 15 V	T_J = 25°C		1		mV
			over the junction temperature range 0°C to 125°C			6	
		LM1117-5.0 I_{OUT} = 0 mA, 6.5 V ≤ V_{IN} ≤ 15 V	T_J = 25°C		1		mV
			over the junction temperature range 0°C to 125°C			10	
ΔV_{OUT}	Load regulation[3]	LM1117-ADJ $V_{IN} - V_{OUT}$ = 3 V, 10 ≤ I_{OUT} ≤ 800 mA	T_J = 25°C		0.2%		
			over the junction temperature range 0°C to 125°C			0.4%	
		LM1117-1.8 V_{IN} = 3.2 V, 0 ≤ I_{OUT} ≤ 800 mA	T_J = 25°C		1		mV
			over the junction temperature range 0°C to 125°C			10	
		LM1117-2.5 V_{IN} = 3.9 V, 0 ≤ I_{OUT} ≤ 800 mA	T_J = 25°C		1		mV
			over the junction temperature range 0°C to 125°C			10	
		LM1117-3.3 V_{IN} = 4.75 V, 0 ≤ I_{OUT} ≤ 800 mA	T_J = 25°C		1		mV
			over the junction temperature range 0°C to 125°C			10	
		LM1117-5.0 V_{IN} = 6.5 V, 0 ≤ I_{OUT} ≤ 800 mA	T_J = 25°C		1		mV
			over the junction temperature range 0°C to 125°C			15	

PARAMETER		TEST CONDITIONS		MIN[1]	TYP[2]	MAX[1]	UNIT
$V_{IN} - V_{OUT}$	Dropout voltage[4]	I_{OUT} = 100 mA	T_J = 25°C		1.1		V
			over the junction temperature range 0°C to 125°C			1.2	
		I_{OUT} = 500 mA	T_J = 25°C		1.15		V
			over the junction temperature range 0°C to 125°C			1.25	
		I_{OUT} = 800 mA	T_J = 25°C		1.2		V
			over the junction temperature range 0°C to 125°C			1.3	
I_{LIMIT}	Current limit	$V_{IN} - V_{OUT}$ = 5 V, T_J = 25°C		800	1200	1500	mA
	Minimum load current[5]	LM1117-ADJ V_{IN} = 15 V	T_J = 25°C		1.7		mA
			over the junction temperature range 0°C to 125°C			5	
	Quiescent current	LM1117-1.8 $V_{IN} \le$ 15 V	T_J = 25°C		5		mA
			over the junction temperature range 0°C to 125°C			10	
		LM1117-2.5 $V_{IN} \le$ 15 V	T_J = 25°C		5		mA
			over the junction temperature range 0°C to 125°C			10	
		LM1117-3.3 $V_{IN} \le$ 15 V	T_J = 25°C		5		mA
			over the junction temperature range 0°C to 125°C			10	
		LM1117-5.0 $V_{IN} \le$ 15 V	T_J = 25°C		5		mA
			over the junction temperature range 0°C to 125°C			10	
	Thermal regulation	T_A = 25°C, 30-ms pulse			0.01	0.1	%/W
	Ripple regulation	f_{RIPPLE} = 1 20 Hz, $V_{IN} - V_{OUT}$ = 3 V V_{RIPPLE} = 1 V_{PP}	T_J = 25°C		75		dB
			over the junction temperature range 0°C to 125°C	60			
	Adjust pin current	T_J = 25°C			60		µA
		over the junction temperature range 0°C to 125°C				120	
	Adjust pin current change	10 ≤ I_{OUT} ≤ 80 0mA, 1.4 V ≤ $V_{IN} - V_{OUT}$ ≤ 10 V	T_J = 25°C		0.2		µA
			over the junction temperature range 0°C to 125°C			5	
	Temperature stability				0.5%		
	Long term stability	T_A = 125°C, 1000 hours			0.3%		
	RMS output noise	(% of V_{OUT}), 10 Hz ≤ f ≤ 10 kHz			0.003%		

Table 10: Electrical Characteristics

6. MICROCONTROLLER

A. MEDIATEK G31 (U108)

Description:

The MT9685xxxxxx is MediaTek's latest SOC solution for UHD smart TV. Based on MediaTek's advanced technologies, the MT9685xxxxxx is integrated with the high-quality video processor which satisfies a variety ofcustomer's requests for image quality to develop the state-of-the-art DTV system. The multi-core CPUs and GPUs deliver high performance for modern Linux and Android TVs. The up-to-date ARM and Mali architecture ensures the best software compatibility. Applications, such as HTML5, Java, Flash, and so on, are implemented with less efforts.

The MediaTek Professional PQ Engine includes all of MediaTek's most advanced color-tuning tools. MediaTek unique color processor with specially-designed color remapping systems assist System-developers to identify PQ characteristics of all the range of panel models quickly and easily. Moreover, MediaTek's innovated UltraClear video processor adopts the new technology for multi-frame video recovery so that contents or details can be restored perfectly and the noises or artifacts from broadcasting or internet can be eliminated.

The MT9685xxxxxx for DTV/MM/OTT applications into a single device, reducing the overall system BOM cost. With versatile peripheral connectivity ports, like HDMI, USB, Ethernet, CVBS, etc., the MT9685xxxxxx can serve as a high-quality media center in home entertainment field.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MT9685xxxxxx has an ultra-low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.

Features:

1. Combo Front-End Demodulators
2. Advanced Multi-Core CPU and 3D GPU
3. 3D Formatter Engine
4. Multi-Standard A/V Format Decoder
5. MediaTek High Performance Video Processor and MediaTek Professional PQ Engine
6. Home Theater Sound Processor
7. Internet and Variety of Connectivity Support
8. Peripheral and Power Management
9. Robust and Efficient Security Engine
10. Full Multi-Media Decoders Including HEVC Decoder Supporting up to UHD/60fps Resolution

High Performance Micro-processor

- ARM Advanced Multi-Core Cortex CPU
- 32KB/32KB I/D cache
- 512KB L3 cache
- Supports Neon instruction sets

3D Graphic GPU

- ARM Advanced Multi-Core Mali GPU
- Vulkan 1.1
- Supports OpenGL ES 3.2/2.0/1.1
- Supports OpenCL 2.0
- Supports DirectX 11 FL9_3
- Supports rendering size up to UHD

Transport Stream De-multiplexer

- Supports two parallel and one serial TS inputs interfaces, with or without sync signal
- Supports one of TS PAD is programmable TS input/output
- Supports external demodulators
- TS data rate is 140Mbit/s for serial and 56MByte/s for parallel
- 128 general purpose PID filters and 128 section filters for all transport stream demultiplexer
- Supports additional audio/video/PCR filters
- Supports time-shift
- Supports 3DES/DES and AES encryption/decryption

MPEG-2 Video Decoder

- ISO/IEC 11172-2 MPEG-1 video format decoding
- ISO/IEC 13818-2 MPEG-2 video MP@HL and HD level
- Supports resolution up to HDTV (1080p60,1080i, 720p) and SDTV
- Supports dual stream decoding for 3D content
- Supports for FHDp60 2x fast forwarding playback

MPEG-4 Video Decoder

- ISO/IEC 14496-2 MPEG-4 ASP video decoding up to HD level
- Supports resolutions up to HDTV
- (1080p@60fps)
- Supports FLV version1 video format decoding
- Supports dual stream decoding for 3D content

H.264 Decoder

- ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 5.2) video decoding
- Supports resolution up to 4096x2160@60fps
- Supports bitrate up to 135Mbps
- Supports resolutions for all DVB, ATSC, HDTV,DVD and VCD
- Supports SVAF 2ES (for Dual Decode)
- Supports MVC 3D decoding up to 1080p@60fps

VP8 Decoder

- Supports Google VP8 decoder
- Supports resolution up to 1920x1080@60fps
- Supports maximum bitrate up to 50Mbps

VP9 Decoder

- Supports Google VP9 decoder
- Supports 4:2:0 subsampling and 8bit/10bit color depth
- Supports max resolution and frame rate 4096x2160@60fps
- Supports max bitrate up to 100Mbps

AV1 Video Decoder

- Supports AV1 video decoding
- Supports Main profile, level 5.1
- Supports 8-bit/10-bit color depth
- Supports resolution up to 4096x2304@60fps
- Supports max bitrate up to 100Mbps

HEVC (H.265) Decoder

- Supports HEVC/H.265 video decoding
- Supports Main/Main-10 profile, and Scalable
- Main/Scalable Main-10 profile, level 5.1, high tier
- Supports 8-bit/10-bit color depth
- Supports resolution up to 4096x2160@60fps, or 4096x2160@60fps+1920x1080@60fps for
- Dolby Vision
- Supports max bitrate upto 100Mbps

H.264 Encoder Optional

- Supports H.264 encoding, Main Profile, level 4.1
- Maximum output frame-rate/resolution: 1920x1080@30fps, 1280x720@60fps

- Supports MVs: 16x16, 16x8, 8x16, 8x4, 4x8, 4x4
- Supports up to quarter-pel
- Supports up to two reference frames

Hardware JPEG Decoder

- Supports upto 1920x1080@30fps,
- 1280x720@60fps
- Supports formats: 422/411/420/444/422T
- Supports scaling down ratios: 1/2x1/2, 1/4x1/4, 1/8x1/8
- Supports both color and grayscale pictures
- Supports sequential mode, single scan
- Supports programmable Region of Interest (ROI)
- Following the file header scan the hardware decoder fully handles the decode process

VC-1 Video Decoder

- Supports SMPTE-421M (VC1 video) decoding up to AP@L3 (2048x1024p60)
- Supports dual stream decoding for 3D content

NTSC/PAL/SECAM Video Decoder

- Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B,D, G, H, M, N, I, Nc), and SECAM standards
- Automatic standard detection
- Motion adaptive 3D comb filter
- Supports CVBS & Y/C S-video inputs
- Supports V-chip

Multi-Standard TV Sound Processor

- Supports BTSC/A2 demodulation
- Supports FM/AM demodulation
- Supports MTS Mode Mono/Stereo/SAP in BTSC mode
- Supports Mono/Stereo/Dual in A2 mode
- Built-in audio sampling rate conversion (SRC)
- Audio processing for loudspeaker channel,including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
- Advanced sound processing options available,for example: Dolby, DTS, DBX-TV
- Supports digital audio format :

MPEG-1, MPEG-2 (Layer I/II), MP3, AAC-LC, HE-AAC, WMA, WMA9 Pro

- Supports Multi-stream programs:

Dolby MS12-B Optional, Dolby MS12-D Optional, Dolby MS12-Y Optional, Dolby MS12-Z Optional, and DTS M6 Optional , DTS M6 multistream decoder/encoder

- Supports Audio Description
- Supports MPEG audio encoding
- Supports time-shifting PVR
- Supports programmable delay for audio/video Synchronization

Audio Interface

- One L/R audio line-input
- One L/R output for main speaker or additional line-output
- Supports stereo headphone driver
- I2S digital audio output and input
- S/PDIF digital audio output and input
- Supports HDMI receiver ARC function
- Supports PDM input for 2/4 channels digital microphone

Analog RGB Compliant Input Ports

- Two analog ports support up to 1080P
- Supports PC RGB input up to SXGA@75Hz
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG Sync-on-Green
- Automatic color calibration

Analog RGB Auto-Configuration & Detection

- Auto input signal format and mode detection
- Auto-tuning function including phasing,positioning, offset and gain configuration
- Sync Detection for H/V Sync

DVI/HDCP/HDMI Compliant Input Ports

- Four HDMI/DVI input ports
- HDMI 2.0b/1.4b Compliant
- HDMI 2.1
- Max bit rate upto 6Gbps in TMDS
- VRR and Dynamic HDR EM packet
- MediaTek iSwitch for fast HDMI switching
- HDCP 2.2/1.4 Compliant
- Supports HDMI CEC
- Supports HDMI ARC/eARC TX

- Robust receiver with excellent long-cable support

MediaTek High Performance Video Processor

- Video Processing Engine
- Supports up to 4K UHD@60p
- 10/12-bit Internal Data Processing
- Arbitrary Frame Rate Conversion
- Video Care Technology
- Video Line Broken Artifact Detection and Removal
- Video Detection & Repairing Technology for Lousy Inputs such as Internet Streaming
- Fully Programmable Multi-Function ScalingEngine
- High-Quality Filters with Programmable Parameter
- An advanced Zoom Algorithm providing Aliasing/Ringing Suppression
- Nonlinear Video Scaling supports various modes including Panorama
- Supports Dynamic Scaling for VC-1
- Fully Programmable Zoom Ratios for Up/Down Scaling
- Independent Horizontal and Vertical Zoom
- Deinterlacer
- Advanced Motion Compensated Video Deinterlacing with Motion Object Stabilizer
- Motion De-Flickering
- Motion Adaptive Deinterlacer
- Edge-Oriented Deinterlacer with Edge Smoothing and Artifact Removal
- Automatic 3:2/2:2/M:N Pull-Down Detection and Recovery
- MediaTek Genuine 3D
- Supports Mandatory 3D Format
- Motion Frame Rate Conversion
- Supports Frame Repeat Frame Rate Conversion
- Supports 4K Motion Compensated Frame Rate Conversion
- Advanced Halo Reduction
- Automatic Film-Mode Detection/Film Judder Cancellation
- Search Range: Big H and V search range to handle fast motion
- Supports Logo Detection and Protection
- Supports Small Object Detection and Protection
- Supports LetterBox
- Backlight Technology
- Supports Direct and Edge Types Local Dimming
- Programmable Light Spread Profile
- Content Adaptive LCD Backlight Control
- High Dynamic Range
- Supports SMPTE ST-2084/ST-2086
- Supports ARIB STD-B67(Hybrid Log Gamma)/BT.2100
- Supports 2094-40 (HDR10 plus)optional
- Supports ITU-R BT.2100
- Ultra HD Premium Ready

— Dolby Vision

- Response Time Compensation
- Supports Overdrive Technology

MediaTek Professional PQ Engine

- UltraClear
- MPEG Artifact Removal
- Advanced Adaptive Block Noise
- Reduction
- Advanced Mosquito Noise Cancellation
- Supports DCR Engine
- UltraClear Noise Reduction
- Ultimate 3D Motion-Compensated Temporal Filtering
- Auto Noise Estimation
- 3D Noise Reduction
- 3D Temporal Noise Reduction for Lousy Air/Cable Input
- S-Powers
- Video Enhancement Processor
- Advanced 3D Independent Multi-Band Control Sharpness Technology
- Advanced Video Enhancement Algorithm provides Aliasing/Ringing Suppression
- Advanced Chroma Transient Improvement
- Supports Luma Transient Improvement
- Super Resolution
- Local Detail Enhancement
- SuperiorClear Multi-Directional

Anti-Aliasing and Jagged Compensation Technology
- SuperiorClear Enhance Management
- MACE
- MediaTek Advanced Color Engine
- MediaTek Graffito Color Manager
- Color Stain Removal Technology
- Standard Color Format and Processing
- Fully Programmable Input/Output
- CSC
- BT601, BT709, BT2020 (CL/NCL)
- xvYCC601, xvYCC709
- AdobeRGB, AdobeYCC601
- sRGB, sYCC601
- Fully Programmable 12-bit RGB Gamma
- Gamut Mapping
- Nonlinear/Linear RGB Domain

Gamut Mapping
- Supports 2D Gamut Mapping
- Supports 3D Gamut Mapping
- Luce
- Contrast Enhancement
- Real-Time Content Adaptive Contrast Enhancement with Chroma Compensated
- Ultra Contrast Dimming
- SDR to HDR

Output Interface
- Single/Dual link 8-bit/10-bit LVDS output
- Supports panel resolution up to Full HD 1920x1080@60Hz (LVDS 2ch)
- 8-lane 8-bit/10-bit Vby1 output (configurable width: 2/4/8 lane)
- Supports panel resolution up to Ultra HD @60Hz (Vby1 8 lane)
- Supports OSD bypass to MTK FRC 120Hz/240Hz chipOptional
- Supports TCON:EPI interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:CMPI interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:ISP interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:CHPI interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:CEDS interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:CSPI interface, panel resolution up to Ultra HD@60Hz
- Supports TTL output, update to 1920x1080@60Hz
- Supports programmable timing controller
- Supports dithering options
- Spread spectrum output frequency for EMI suppression
- Supports 60Hz 3D polarizd panel (line interleave)
- Supports Cinema output mode

CVBS Video Encoder
- Supports all NTSC/PAL TV Standard
- Stand-alone scaling engine (no vertical scaling up)
- Programmable Hue, Contract, Brightness
- Supports WSS output

CVBS Video Output
- Allows CVBS output of digital content to SCART

2D Graphics Engine
- Hardware Graphics Engine for responsive interactive applications
- Supports line draw, rectangle draw/fill and text draw
- Supports BitBlt, Stretch BitBlt, Italic Bitblt,Mirror BitBlt and Rotate BitBlt
- Supports alpha-blending operation
- Supports source/destination color key and alpha key
- Supports dither
- Supports color format conversion and format transformation
- Raster Operation (ROP)
- Supports DFB and Porter-Duff operation

VIF Demodulator
- Compliant with NTSC M/N, PAL B, G/H, I, D/K,SECAM L/L' standards
- Supports low IF architecture
- Audio/Video internal dual-path processor
- Locking range improvement

ATSC/QAM Demodulator

- ATSC A/53 compliant 8VSB
- ITU-T J.83 Annex B, SCTE DVS-031 compliant 64/256QAM receiver
- 2010 - A74 compliant
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- Integrated deinterleaver RAM for Level 1 J =1 and Level 2 J= 1,2,3.4
- Supports LIF interfaces

DVB-C Demodulator

- Compliant with ITU J.83 Annex A/C DVB-C (EN 300 429)
- Supports 1-7.2 M Baud symbol rate
- Automatic blind channel scan (constellation and symbol rate)
- Supports LIF interfaces
- IIS performance improvement

DVB-T Demodulator

- Compliant with DVB-T (ETSI EN 300 744)
- Nordig 2.2.2, D-book 7.0 compliant
- Accept low IF inputs in 6, 7, 8MHz channel bandwidths
- Supports all guard intervals (1/32 to 1/4)
- Supports all constellations (QPSK, 16-QAM, 64-QAM)
- Ultra fast automatic blind UHF/VHF channel scan
- Optimized for SFN channels with pre/postcursive echoes inside/outside the guard
- Phase-Noise suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel interference suppression
- CNR performance improvement
- Outside-GI performance improvement

DVB-T2 Demodulator

- Compliant with DVB-T2 (ETSI EN 302 755) v1.3.1, T2-base & T2-Lite profile
- Nordig Unified 2.2.2, D-Book 7.0 compliant
- Supports all guard intervals (1/128 to 1/4)
- Supports all FFT modes from 1K to 32K
- Supports all long and short block code rates (1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 2/5, 1/3)
- Supports all constellations (QPSK, 16-QAM,64-QAM, 256-QAM)
- Transmit diversity (MISO) support
- Supports all scattered pilot patterns (PP1 to PP8)
- Supports rotated and non-rotated constellations
- Supports single and multiple PLPs
- Accept low IF inputs in 1.7, 5, 6, 7, 8MHz channel bandwidths
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- Outside GI improvement
- Locking time improvement

DVB-S Demodulator

- Compliant with DVB-S (ETSI EN 300 421)
- Data Rate: 1-70 Msps
- Code Rates: 1/2, 2/3, 3/4, 5/6, 7/8
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors
- Improved CNR performance

DVB-S2 Demodulator

- Compliant with DVB-S2 (ETSI EN 302 307)
- Data Rate: 1-70 Msps for QPSK , 8PSK, 16APSK,

1-57 sps for 32APSK

- Constellations: QPSK , 8PSK , 16APSK and 32APSK

- QPSK Code Rates: 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
- 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9, 9/10
- 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
- 32APSK Code Rates: 3/4, 4/5, 5/6, 8/9, 9/10

- Supports CCM and VCM
- Supports Single Transport Stream and Multiple Transport Streams
- Roll-off factors for pulse shaping: 0.2, 0.25, and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors

DVB-S2X Demodulator

- Compliant with DVB-S2 Extensions (ETSI EN302 307-2, Broadcast services except for Channel Bonding)
- Data Rate: 1-70 Msps for QPSK , 8PSK, 8APSKL,16APSK, 16APSK-L, 1-57 Msps for 32APSK, and 32APSK-L
- Constellations: QPSK , 8PSK, 8APSK-L, 16APSK,16APSK-L, 32APSK, and 32APSK-L

- QPSK Code Rates: 1/4, 1/3, 2/5, 1/2, 3/5,2/3, 3/4, 4/5, 5/6, 8/9, 9/10, 13/45, 9/20,11/20
- 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9,9/10, 23/36, 25/36, 13/18
- 8APSK-L Code Rates: 5/9, 26/45
- 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9,9/10, 26/45, 3/5, 28/45, 23/36, 25/36,13/18, 7/9, 77/90
- 16APSK-L Code Rates: 5/9, 8/15, 1/2, 3/5,2/3
- 32APSK Code Rates: 3/4, 4/5, 5/6, 8/9,9/10, 32/45, 11/15, 7/9
- 32APSK-L Code Rates: 2/3

- Supports CCM and VCM
- Supports Single Transport Stream and Multiple Transport Streams
- Roll-off factors for pulse shaping: 0.05, 0.1, 0.15, 0.2, 0.25, and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors

Connectivity

- Three USB 2.0 host ports
- USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting
- Embedded 10/100 Ethernet PHY
- Supports Ethernet Wake-On-Lan

Miscellaneous

- DRAM interface supports DDR3
- Supports PVR
- Parallel interface for external parallel eMMC flash and NAND flash support
- Power control module with ultra low power MCU available in standby mode

- 542-ball BGA package

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V_{VDD_33}		TBD		V
1.5V Supply Voltages (DDR3)	V_{VDD_15}		TBD		V
Core Supply Voltages	V_{VDD_core}		TBD		V
CPU Supply Voltages	V_{VDD_cpu}		TBD		V
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

Table 11: Recommended Operating Conditions

B. MEDIATEK G32 (U108)

The MT9675xxxxxx is MediaTek's latest SOC solution for UHD smart TV. Based on MediaTek's advanced technologies, the MT9675xxxxxx is integrated with the high-quality video processor which satisfies a variety of customer's requests for image quality to develop the state-of-the-art DTV system. The multi-core CPUs and GPUs deliver high performance for modern Linux and Android TVs. The up-to-date ARM and Mali architecture ensures the best software compatibility.

Applications, such as HTML5, Java, Flash, and so on, are implemented with less efforts.

The MediaTek Professional PQ Engine includes all of MediaTek's most advanced color-tuning tools. MediaTek unique color processor with specially-designed color remapping systems assist System-developers to identify PQ characteristics of all the range of panel models quickly and easily.

The MT9675xxxxxx for DTV/MM/OTT applications into a single device, reducing the overall system BOM cost. With versatile peripheral connectivity ports, like HDMI, USB, Ethernet, CVBS, etc., the MT9675xxxxxx can serve as a high-quality media center in home entertainment field.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MT9675xxxxxx has an ultra-low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.

MT9675xxxxxx is a highly integrated smart TV solution, which supports LVDS/Vby1 output, DTV channel decoding, MPEG decoding, AV1 decoding, and security OS. MT9675xxxxxx serves full functions of multi-media centers with a high performance CPU, GPU, and AV CODEC/security engines.

1. Combo Front-End Demodulators
2. Advanced Multi-Core CPU and 3D GPU
3. 3D Formatter Engine
4. Multi-Standard A/V Format Decoder
5. MediaTek High Performance Video Processor and MediaTek Professional PQ Engine
6. Home Theater Sound Processor
7. Internet and Variety of Connectivity Support
8. Peripheral and Power Management

9. Robust and Efficient Security Engine
10. Full Multi-Media Decoders Including AV1/ HEVC Decoder Supporting up to FHD/60fps Resolution

High Performance Micro-processor
- ARM Advanced Multi-Core Cortex PU
- 32KB/32KB I/D cache
- 512KB L2 cache
- Supports Neon instruction sets

3D Graphic GPU
- ARM Advanced Multi-Core Mali GPU
- Vulkan 1.1
- Supports OpenGL ES 3.2/2.0/1.1
- Supports OpenCL 2.0
- Supports DirectX 11 FL9_3
- Supports rendering size up to UHD

Transport Stream De-multiplexer
Supports two parallel and one serial TS inputs interfaces, with or without sync signal
- Supports one of TS PAD is programmable TS input/output
- Supports external demodulators
- TS data rate is 140Mbit/s for serial and 56MByte/s for parallel
- 128 general purpose PID filters and 128 section filters for all transport stream demultiplexer
- Supports additional audio/video/PCR filters
- Supports time-shift
- Supports 3DES/DES and AES encryption/decryption

MPEG-2 Video Decoder
- ISO/IEC 11172-2 MPEG-1 video format decoding
- ISO/IEC 13818-2 MPEG-2 video MP@HL and HD level
- Supports resolution up to HDTV (1080p60,1080i, 720p) and SDTV
- Supports dual stream decoding for 3D content
- Supports for FHDp60 2x fast forwarding playback

MPEG-4 Video Decoder
- ISO/IEC 14496-2 MPEG-4 ASP video decoding up to HD level
- Supports resolutions up to HDTV (1080p@60fps)
- Supports Divx Home Theater & HD profiles
- Supports FLV version1 video format decoding
- Supports dual stream decoding for 3D content

H.264 Decoder
- ITU-T H.264, ISO/IEC 14496-10(main and high profile up to level 5.2) video decoding
- Supports resolutions up to 4096x2160@fps
- Supports bitrate up to 135Mbps
- Supports resolutions for all DVB, ATSC, HDTV,DVD and VCD
- Supports SVAF 2ES (for Dual Decode)
- Supports MVC 3D decoding up to 1080p@60fps

VP8 Decoder
- Supports Google VP8 decoder
- Supports resolution up to 1920x1080@60fps
- Supports maximum bitrate up to 50Mbps

VP9 Decoder
- Supports Google VP9 decoder
- Supports 4:2:0 subsampling and 8bit/10bit color depth
- Supports max resolution and frame rate 4096x2160@60fps
- Supports max bitrate up to 100Mbps

AVS+ DecoderOptional
- Supports Broadcasting profile,level 6.0.1.08.60(AVS+)
- Supports Jizhun profile, level 6.0
- Supports bitrate up to 50Mbps
- Supports resolution up to 1920x1080@60fps
- Supports dual stream decoding

AVS2 DecoderOptional
- Supports AVS2 video decoding
- Supports Main-10bit profile, level 8.2.60
- Supports 8-bit/10-bit color depth
- Supports resolution up to 4096x2304@60fps
- Supports max bitrate up to 100Mbps

AV1 Video Decoder Optional

- Supports AV1 video decoding
- Supports Main profile, level 5.1
- Supports 8-bit/10-bit color depth
- Supports resolution up to 4096x2304@60fps
- Supports max bitrate up to 100Mbps

LZMA Compression

- Supports ACP interface
- Supports LZMA proprietary format
- Supports fixed 4KB
- Supports Input data rate 56MB/s
- Supports Output data rate 133MB/s
- Supports Command Queue

RealMedia DecoderOptional

- Supports RV8, RV9, RV10 decoders
- Supports file formats with RM and RMVB
- Supports maximum resolution up to 1080p@60fps
- Supports Picture Re-sampling
- Supports in-loop de-block for B-frame
- Supports dual stream decoding

HEVC (H.265) Decoder

- Supports HEVC/H.265 video decoding
- Supports Main/Main-10 profile, and Scalable Main/Scalable Main-10 profile, level 5.1, hightier
- Supports 8-bit/10-bit color depth
- Supports resolution up to 4096x2160@75fps,or 4096x2160@60fps+1920x1080@60fps for Dolby Vision
- Supports max bitrate upto 100Mbps

H.264 EncoderOptional

- Supports H.264 encoding, Main Profile, level 4.1
- Maximum output frame-rate/resolution:1920x1080@30fps, 1280x720@60fps
- Supports MVs: 16x16, 16x8, 8x16, 8x4, 4x8,4x4
- Supports up to quarter-pel
- Supports up to two reference frames

Hardware JPEG Decoder

- Supports upto 1920x1080@30fps, 1280x720@60fps
- Supports formats: 422/411/420/444/422T
- Supports scaling down ratios: 1/2x1/2, 1/4x1/4, 1/8x1/8
- Supports both color and grayscale pictures
- Supports sequential mode, single scan
- Supports programmable Region of Interest(ROI)
- Following the file header scan the hardware decoder fully handles the decode process

VC-1 Video DecoderOptional

- Supports SMPTE-421M (VC1 video) decoding up to AP@L3 (2048x1024p60)
- Supports dual stream decoding for 3D content

NTSC/PAL/SECAM Video Decoder

- Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B,D, G, H, M, N, I, Nc), and SECAM standards
- Automatic standard detection
- Motion adaptive 3D comb filter
- Supports CVBS & Y/C S-video inputs
- Supports Teletext and V-chip

Multi-Standard TV Sound Processor

- Supports BTSC/A2 demodulation
- Supports NICAM/FM/AM demodulation
- Supports MTS Mode Mono/Stereo/SAP inBTSC mode
- Supports Mono/Stereo/Dual in A2/NICAM mode
- Built-in audio sampling rate conversion (SRC)
- Audio processing for loudspeaker channel,including volume, balance, mute, tone, EQ,virtual stereo/surround and treble/bass controls
- Advanced sound processing options available,for example: Dolby1, DTS2, DBX-TV3
- Supports digital audio format : MPEG-1, MPEG-2 (Layer I/II), MP3, AAC-LC, HE-AAC, WMA, WMA9 Pro
- Supports Multi-stream programs : Dolby MS12-B **Optional**, Dolby MS12-D **Optional**,

Dolby MS12-Y **Optional**,
Dolby MS12-Z **Optional**,
and DTS M6 **Optional**,
DTS M6 multistream decoder/encoder

- Supports Audio Description
- Supports MPEG audio encoding
- Supports time-shifting PVR
  - Trademark of Dolby Laboratories
  - Trademark of DTS, Inc.Optional Please see Ordering Guide for details
  - Trademark of DBX-TV, Inc.
- Supports programmable delay for audio/video synchronization

Audio Interface

- One L/R audio line-input
- One L/R output for main speaker or additional line-output
- Supports stereo headphone driver
- I2S digital audio output and input
- S/PDIF digital audio output and input **optional**
- Supports HDMI receiver ARC function
- Supports PDM input for 2/4 channels digital microphone

Analog RGB Compliant Input Ports

- Two analog ports support up to 1080P
- Supports PC RGB input up to SXGA@75Hz
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG Sync-on-Green
- Automatic color calibration

Analog RGB Auto-Configuration & Detection

- Auto input signal format and mode detection
- Auto-tuning function including phasing,positioning, offset and gain configuration
- Sync Detection for H/V Sync

DVI/HDCP/HDMI Compliant Input Ports

- Four HDMI/DVI input ports
- HDMI 2.0b/1.4b Compliant
- HDMI 2.1
  - Max bit rate upto 6Gbps in TMDS
  - VRR and Dynamic HDR EM packet
- MediaTek iSwitch for fast HDMI switching
- HDCP 2.2/1.4 Compliant
- Supports HDMI CEC
- Supports HDMI ARC TX
- Robust receiver with excellent long-cable support

MediaTek High Performance Video Processor

- Video Processing Engine
  - Supports up to 4K UHD@60p
  - 10/12-bit Internal Data Processing
  - Arbitrary Frame Rate Conversion
- Video Care Technology
  - Video Line Broken Artifact Detection and Removal
  - Video Detection & Repairing Technology for Lousy Inputs such as Internet Streaming
- Fully Programmable Multi-Function Scaling Engine
  - High-Quality Filters with Programmable Parameter
  - An advanced Zoom Algorithm providing Aliasing/Ringing Suppression
  - Nonlinear Video Scaling supports various modes including Panorama
  - Supports Dynamic Scaling for RM, VC-1
  - Fully Programmable Zoom Ratios for Up/Down Scaling
  - Independent Horizontal and Vertical Zoom
- Deinterlacer
  - Motion Compensated Video Deinterlacing with Motion Object Stabilizer
  - Motion Adaptive Deinterlacer
  - Edge-Oriented Deinterlacer with Edge Smoothing and Artifact Removal
  - Automatic 3:2/2:2/M:N Pull-Down Detection and Recovery
- MediaTek Genuine 3D
  - Supports Mandatory 3D Format
- Backlight Technology
  - Supports Direct and Edge Types Local
- Dimming
  - Programmable Light Spread Profile
  - Content Adaptive LCD Backlight Control
- High Dynamic Range
  - Supports SMPTE ST-2084/ST-2086
  - Supports ARIB STD-B67(Hybrid Log Gamma)/BT.2100
  - Supports 2094-40 (HDR10 plus)

- Supports ITU-R BT.2100
- Ultra HD Premium Ready
- Dolby Vision

- Response Time Compensation
  - Supports Overdrive Technology

MediaTek Professional PQ Engine

- UltraClear

− MPEG Artifact Removal

- Advanced Adaptive Block Noise Reduction
- Advanced Mosquito Noise Cancellation

− UltraClear Noise Reduction

- 3D Motion-Estimation Temporal Filtering

− 3D Noise Reduction

- 3D Temporal Noise Reduction for Lousy Air/Cable Input
- S-Powers

− Video Enhancement Processor

- Advanced 3D Independent Multi-Band Control Sharpness Technology
- Advanced Video Enhancement Algorithm providesAliasing/Ringing Suppression
- Advanced Chroma Transient Improvement
- Supports Luma Transient Improvement
  - Super Resolution
- Local Detail Enhancement
- SuperiorClear Multi-Directional Anti-Aliasing and Jagged Compensation Technology
- SuperiorClear Enhance Management
- MACE
  - MediaTek Advanced Color Engine
- MediaTek Graffito Color Manager
- Color Stain Removal Technology
  - Standard Color Format and Processing
- Fully Programmable Input/Output CSC
- BT601, BT709, BT2020 (CL/NCL)
- xvYCC601, xvYCC709
- AdobeRGB, AdobeYCC601
- sRGB, sYCC601
- Fully Programmable 12-bit RGB Gamma
  - Gamut Mapping
- Nonlinear/Linear RGB Domain Gamut Mapping
- Supports 2D Gamut Mapping
- Supports 3D Gamut Mapping
- Luce
  - Contrast Enhancement
- Real-Time Content Adaptive Contrast Enhancement with Chroma Compensated
- Ultra Contrast Dimming
  - SDR to HDR

Output Interface

- Single/Dual link 8/10-bit LVDS output
- Supports panel resolution up to Full HD 1920x1080@60Hz (LVDS 2ch)
- 8 lane 8/10-bit Vby1 output (configurable width: 2/4/8 lane)
- Supports panel resolution up to Ultra HD@60Hz (Vby1 8 lane)
- Supports OSD bypass to MTK FRC 120Hz/240Hz chip Optional
- Supports TCON:miniLVDS 4ch interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:EPI interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:CMPI interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:ISP interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:CHPI interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:CEDS interface, panel resolution up to Ultra HD@60Hz
- Supports TCON:CSPI interface, panel resolution up to Ultra HD@60Hz
- Supports TTL output, update to 1920x1080@60Hz
- Supports programmable timing controller
- Supports dithering options
- Spread spectrum output frequency for EMI suppression
- Supports 60Hz 3D polarizd panel (line interleave)
- Supports Cinema output mode

CVBS Video Encoder

- Supports all NTSC/PAL TV Standard
- Stand-alone scaling engine (no vertical scaling up)
- Programmable Hue, Contract, Brightness
- Supports TTX/WSS output

CVBS Video Output

- Allows CVBS output of digital content to SCART

2D Graphics Engine

- Hardware Graphics Engine for responsive interactive applications
- Supports line draw, rectangle draw/fill and text draw Supports BitBlt, Stretch BitBlt, Italic Bitblt,Mirror BitBlt and Rotate BitBlt
- Supports alpha-blending operation
- Supports source/destination color key and alpha key
- Supports dither
- Supports color format conversion and format transformation
- Raster Operation (ROP)
- Supports DFB and Porter-Duff operation

VIF Demodulator

- Compliant with NTSC M/N, PAL B, G/H, I, D/K, SECAM L/L' standards
- Supports low IF architecture
- Audio/Video internal dual-path processor
- Locking range improvement

ATSC/QAM Demodulator

- ATSC A/53 compliant 8VSB
- ITU-T J.83 Annex B, SCTE DVS-031 compliant 64/256QAM receiver
- 2010 - A74 compliant
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- Integrated deinterleaver RAM for Level 1 J =1 and Level 2 J= 1,2,3.4
- Supports LIF interfaces

ISDB-T DemodulatorOptional

- Compliant with ISDB-T ARIB STD-B31
- Compliant with ISDB-Tsb ARIB STD-B29
- Supports all modes defined in ISDB-T specs
- Supports all guard ratios: 1/4, 1/8, 1/16, 1/32
- Support LIF interfaces
- Impulse-noise suppression
- Phase noise compensation
- Outside-GI performance improvement
- CNR performance improvement

DVB-C Demodulator

- Compliant with ITU J.83 Annex A/C DVB-C (EN300 429)
- Supports 1-7.2 M Baud symbol rate
- Automatic blind channel scan (constellation and symbol rate)
- Supports LIF interfaces
- IIS performance improvement

DVB-T Demodulator

- Compliant with DVB-T (ETSI EN 300 744)
- Nordig 2.2.2, D-book 7.0 compliant
- Accept low IF inputs in 6, 7, 8MHz channel bandwidths
- Supports all guard intervals (1/32 to 1/4)
- Supports all constellations (QPSK, 16-QAM,64-QAM)
- Ultra fast automatic blind UHF/VHF channel scan
- Optimized for SFN channels with pre/postcursive echoes inside/outside the guard
- Phase-Noise suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel interference suppression
- CNR performance improvement
- Outside-GI performance improvement

DVB-T2 DemodulatorOptional

- Compliant with DVB-T2 (ETSI EN 302 755) v1.3.1, T2-base & T2-Lite profile
- Nordig Unified 2.2.2, D-Book 7.0 compliant
- Supports all guard intervals (1/128 to 1/4)
- Supports all FFT modes from 1K to 32K
- Supports all long and short block code rates(1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 2/5, 1/3)
- Supports all constellations (QPSK, 16-QAM,64-QAM, 256-QAM)
- Transmit diversity (MISO) support
- Supports all scattered pilot patterns (PP1 toPP8)

- Supports rotated and non-rotated constellations
- Supports single and multiple PLPs
- Accept low IF inputs in 1.7, 5, 6, 7, 8MHz channel bandwidths
- All digital demodulation and timing recovery loops for tracking frequency and clock offset.
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- Outside GI improvement
- Locking the improvement

DVB-S DemodulatorOptional

- Compliant with DVB-S (ETSI EN 300 421)
- Data Rate: 1-70 Msps
- Code Rates: 1/2, 2/3, 3/4, 5/6, 7/8
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors
- Improved CNR performance

DVB-S2 DemodulatorOptional

- Compliant with DVB-S2 (ETSI EN 302 307)
- Data Rate: 1-70 Msps for QPSK , 8PSK, 16APSK,1-57 Msps for 32APSK
- Constellations: QPSK , 8PSK , 16APSK and 32APSK
  - QPSK Code Rates: 1/2, 3/5, 2/3, 3/4, 4/5,5/6, 8/9, 9/10
  - 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9,9/10
  - 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9,9/10
  - 32APSK Code Rates: 3/4, 4/5, 5/6, 8/9,9/10
- Supports CCM and VCM
- Supports Single Transport Stream and Multiple Transport Streams
- Roll-off factors for pulse shaping: 0.2, 0.25,and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors

DVB-S2X DemodulatorOptional

- Compliant with DVB-S2 Extensions (ETSI EN302 307-2, Broadcast services except for Channel Bonding)
- Data Rate: 1-70 Msps for QPSK , 8PSK, 8APSK-L,16APSK, 16APSK-L, 1-57 Msps for 32APSK, and 32APSK-L
- Constellations: QPSK , 8PSK, 8APSK-L, 16APSK,16APSK-L, 32APSK, and 32APSK-L
  - QPSK Code Rates: 1/4, 1/3, 2/5, 1/2, 3/5,2/3, 3/4, 4/5, 5/6, 8/9, 9/10, 13/45, 9/20,11/20
  - 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9,9/10, 23/36, 25/36, 13/18
  - 8APSK-L Code Rates: 5/9, 26/45
  - 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9,9/10, 26/45, 3/5, 28/45, 23/36, 25/36,13/18, 7/9, 77/90
  - 16APSK-L Code Rates: 5/9, 8/15, 1/2, 3/5,2/3
  - 32APSK Code Rates: 3/4, 4/5, 5/6, 8/9,9/10, 32/45, 11/15, 7/9
  - 32APSK-L Code Rates: 2/3
- Supports CCM and VCM

- Supports Single Transport Stream and Multiple Transport Streams
- Roll-off factors for pulse shaping: 0.05, 0.1, 0.15, 0.2, 0.25, and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and carrier frequencies
- Equalizer compensates for channel impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon limit performances
- Integrated signal quality and BER monitors

Connectivity

- Three USB 2.0 host ports
- USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting
- Embedded 10/100 Ethernet PHY
- Supports Ethernet Wake-On-Lan

Miscellaneous

- DRAM interface support DDR3/4
- Supports PVR
- Parallel interface for external parallel eMMC flash and NAND flash support
- Power control module with ultra low power MCU available in standby mode
- 542-ball BGA package
- Operating Voltages: TBD

Recommended Operating Condition:

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V_{VDD_33}	3.14	3.3	3.46	V
1.5V Supply Voltages (DDR3)	V_{VDD_15}	1.43	1.5	1.57	V
Core Supply Voltages	V_{VDD_core}		TBD		V
			TBD		V
CPU Supply Voltages	V_{VDD_cpu}		TBD		V
			TBD		V
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

Table 12: Recommended Operating Conditions

Absolute Maximum Ratings:

Parameter	Symbol	Min	Max	Unit
3.3V Supply Voltages	V_{VDD_33}		3.63	V
1.5V Supply Voltages	V_{VDD_15}		1.65	V
Core Supply Voltages	V_{VDD_core}		TBD	V
CPU Supply Voltages	V_{VDD_cpu}		TBD	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$		5.3	V
Input Voltage (non 5V tolerant inputs)	V_{IN}		V_{VDD_33}	V
Storage Temperature	T_{STG}	-40	150	°C

Table 13: Absolute Maximum Ratings

7. EMMC

A. SAMSUNG EMMC 8GB KLM8G1GETF-B041 BGA153 (U103)

Description:

SAMSUNG eMMC is an embedded MMC solution designed in a BGA package form. eMMC operation is identical to a MMC device and therefore is a simple read and write to memory using MMC protocol v5.1 which is a industry standard. eMMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF or VCC) whereas 1.8V or 3V dual supply voltage (VDD or VCCQ) is supported for the MMC controller. SAMSUNG eMMC supports HS400 in order to improve sequential bandwidth, especially sequential read performance. There are several advantages of using eMMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market. The embedded flash management software or FTL (Flash Transition Layer) of eMMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

Key Features:

- Embedded MultiMediaCard Ver. 5.1 compatible.
- SAMSUNG eMMC supports features of eMMC5.1 which are defined in JEDEC Standard
  - Major Supported Features : HS400, Field Firmware Update, Cache, Command Queuing, Enhanced Strobe Mode, Secure Write Protection, Partition types
  - Non-supported Features : Large Sector Size (4KB)
- Backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-eMMC systems)
- Data bus width : 1bit (Default), 4bit and 8bit
- MMC I/F Clock Frequency : 0 ~ 200MHz
- MMC I/F Boot Frequency : 0 ~ 52MHz

- Temperature : Operation (-25°C ~ 85°C), Storage without operation (-40°C ~ 85°C)
- Power : Interface power →VCCQ(1.70V ~ 1.95V), Memory power → VCC(2.7V~ 3.6V)

Item	Min	Max	Unit
V_{CCQ}	1.70	1.95	V
V_{CC}	2.7	3.6	V
V_{SS}	-0.5	0.5	V

Table 14: Supply Voltage

B. SAMSUNG EMMC 16GB KLMAG1JETDB041 FBGA153 (U103)

Description:

SAMSUNG eMMC is an embedded MMC solution designed in a BGA package form. eMMC operation is identical to a MMC device and therefore is a simple read and write to memory using MMC protocol v5.1 which is a industry standard. eMMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF or VCC) whereas 1.8V or 3V dual supply voltage (VDD or VCCQ) is supported for the MMC controller. SAMSUNG eMMC supports HS400 in order to improve sequential bandwidth, especially sequential read performance. There are several advantages of using eMMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market. The embedded flash management software or FTL (Flash Transition Layer) of eMMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

Key Features:

- Embedded MultiMediaCard Ver. 5.1 compatible.
- SAMSUNG eMMC supports features of eMMC5.1 which are defined in JEDEC Standard
  - Major Supported Features : HS400, Field Firmware Update, Cache, Command Queuing, Enhanced Strobe Mode, Secure Write Protection, Partition types
  - Non-supported Features : Large Sector Size (4KB)
- Backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-eMMC systems)
- Data bus width : 1bit (Default), 4bit and 8bit
- MMC I/F Clock Frequency : 0 ~ 200MHz
- MMC I/F Boot Frequency : 0 ~ 52MHz
- Temperature : Operation (-25°C ~ 85°C), Storage without operation (-40°C ~ 85°C)
- Power : Interface power →VCCQ(1.70V ~ 1.95V), Memory power → VCC(2.7V~ 3.6V)

Item	Min	Max	Unit
V_{CCQ}	1.70	1.95	V
V_{CC}	2.7	3.6	V
V_{SS}	-0.5	0.5	V

Table 15: Supply Voltage

8. USB INTERFACE

USB POWER SWITCH ADJ SAFE JW7111SOTB SOT23-6 (U115-U116)

Description:

TheJW® 7115 series and JW7111 are allsingle channel current-limited power switch optimized for Universal Serial Bus (USB) and other hot-swap applications. The rise and fall times are controlled to minimize current overshoot or undershoot during switches on/off. The device has fast short-circuit response time for improved overall system robustness. It provides a complete protection solution, such asover-currentprotection, over-temperature protection and short-circuit protection, as well ascontrolled rise time and under-voltage lockout function. A7.5ms de-glitch time on the open-drain Flag output prevents falseover-current reporting. JW7115 Series offerSOT23-5 package.JW7111 offers both DFN2X2-6 and SOT23-6 packages.

Features:

- 50mΩ Integrated N-MOSFET Switch
- Accurate Current Limit
- FLG: active low
- Constant-Current During Over-Current
- Fast Short-Circuit Response Time: 2μs (typ.)
- Operating Range: 2.7V - 5.5V
- Built-in Soft-Start with 3ms Typical Rise Time
- Over-Current, Output Over-Voltage and Thermal Protection
- Fault Report (FAULT) with De-glitch Time
- UL Recognized, File Number E497605
- IEC Recognized, File Number DK-69902-UL
- ESD Protection: 2kV HBM, 500V CDM
- Available in SOT23-5, SOT23-6 and DFN2X2-6Packages

Applications:

- Set-Top Boxes
- LCD TVs & Monitors
- Residential Gateways
- Laptops, Desktops, Servers, e-books, Printers, Docking
- Stations, HUBs

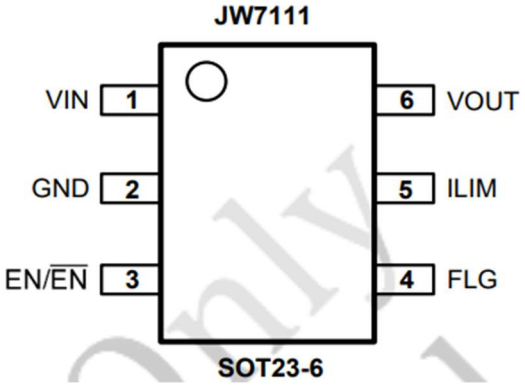


Figure 21: Pin Description

Pin Description:

Pin			Name	Description
SOT23-5	SOT23-6	DFN2X2-6		
1	6	1	VOUT	Output voltage
2	2	5	GND	Ground(0V)
3	4	3	FLG	Active-low open-drain output, asserted during overcurrent, over-temperature.
4	3	4	EN/$\overline{EN}$	Enable input JW7115/JW7115-1/JW7115-2/JW7111: logic high turns on power switch. JW7115A/JW7115A-1/JW7115A-2/JW7111A: logic low turns on power switch.
5	1	6	VIN	Input, connect a 0.1μF or greater ceramic capacitor from VIN to GND as close to IC as possible.
-	5	2	ILIM	Use external resistor to set current-limit threshold; Recommended 10kΩ≦R_{LIM}≦232kΩ.

Absolute Maximum Ratings:

V_{IN} PIN	-0.3V to 6.5V
V_{OUT} PIN	-0.3V to 6.5V
Other Pins Voltage	-0.3V to 6.5V
I_{LIM} Source Current	1mA
Junction Temperature	150ºC
Lead Temperature	260ºC
Storage Temperature	-65ºC to +150ºC

Table 16: Pin Description & Absolute Maximum Ratings

Recommended Operating Conditions:

V_{IN} PIN	2.7V to 5.5V
V_{OUT} PIN	0V to (V_{IN}+0.2V)
EN/$\overline{EN}$ PIN Voltage	0V to 5.5V
High-Level Input Voltage on EN/$\overline{EN}$	1.4V to V_{IN}
Low-Level Input Voltage on EN/$\overline{EN}$	0V to 0.5V
Operating Junction Temperature	-40ºC to +125ºC

Table 17: Recommended Operating Conditions

Electrical Characteristics:

TA = +25 ℃, VIN = 2.7V to 5.5V, V_{EN} = 0V or V_{EN} = VIN, unless otherwise stated.							
Item	**Symbol**	**Condition[5)]**		**Min.**	**Typ.**	**Max.**	**Units**
Supply							
Input UVLO	V_{UVLO}	VIN Rising			2.4	2.65	V
Input UVLO Hysteresis	ΔV_{UVLO}	VIN Decreasing			25		mV
Input Shutdown Current	I_{SHDN}	VIN= 5.5V, Disabled, VOUT = Open			0.1	1	uA
Input Quiescent Current	I_Q	VIN= 5.5V, Enabled, VOUT = Open			80	130	uA
Power Switch							
Switch On-Resistance	$R_{DS(ON)}$	SOT2x3-5	T_J = +25 ℃, VIN= 5.0V		50	55	mΩ
			-40°C ≤ T_A ≤ +85°C			60	
		SOT23-6	T_J = +25 ℃, VIN= 5.0V		50	55	
			-40°C ≤ T_A ≤ +85°C			60	
		DFN2X2-6	T_J = +25 ℃, VIN= 5.0V		50	60	
			-40°C ≤ T_A ≤ +85°C			75	
Output Turn-On Rise Time	t_R	VIN= 5.5V, C_L = 1μF, R_{LOAD} = 100Ω. Figure 1.			1.1	1.5	ms
		VIN= 2.7V, C_L = 1μF, R_{LOAD} = 100Ω.			0.7	1	
Output Turn-Off Fall Time	t_F	VIN= 5.5V, C_L = 1μF, R_{LOAD} = 100Ω.e Figure 1.		0.1		0.5	ms
		VIN= 2.7V, C_L = 1μF, R_{LOAD} = 100Ω.		0.1		0.5	
Current Limit							
Current-Limit Threshold (maximum DC output current), VOUT = VIN -0.5V	I_{LIMIT}	JW7115/ JW7115A	-40°C ≤ T_A ≤+85°C	3	3.3	3.6	A
		JW7115-2/ JW7115A-2		2.0	2.2	2.4	
		JW7115-1/ JW7115A-1		1.1	1.3	1.5	
		JW7111/ JW7111A	R_{LIM} = 10kΩ, -40 ℃ ~+85 ℃	2.2	2.365	2.542	
			R_{LIM} = 15kΩ, -40 ℃ ~+85 ℃	1.54	1.632	1.73	
			R_{LIM} = 20kΩ, T_J = +25 ℃	1.18	1.251	1.326	
			R_{LIM} = 20kΩ, -40 ℃ ~+85 ℃	1.16	1.251	1.340	
			R_{LIM}= 49.9kΩ, T_J = +25 ℃	0.5	0.530	0.562	
			R_{LIM}= 49.9kΩ, -40 ℃ ~+85 ℃	0.485	0.529	0.573	
			R_{LIM} = 210kΩ	0.121	0.142	0.162	
			I_{LIMIT} Shorted to VIN	0.05	0.75	0.100	
			I_{LIMIT} Shorted to GND	2.2	2.365	2.542	

Short-Circuit Current Limit, VOUT Connected to GND[7]	I_{SHORT}	JW7115/ JW7115A			3.2		A
		JW7115-1/ JW7115A-1			1.3		
		JW7115-2/ JW7115A-2			2.2		
		JW7111/ JW7111A	R_{LIM} = 10kΩ		2.62		A
			R_{LIM} = 15kΩ		1.82		
			R_{LIM} = 20kΩ		1.38		
			R_{LIM} = 49.9kΩ		0.57		
Short-Circuit Response Time	t_{SHORT}	VOUT= 0V to I_{OUT} = I_{LIMIT}(VOUT shorted to ground). See Figure 2.			2		μs
Enable Pin							
EN/$\overline{EN}$ Input Leakage Current	$I_{LEAK-EN}$	VIN= 5V, V_{EN} = 0V and 6V		-0.5		0.5	uA
Turn-On Time	t_{ON}	C_L = 1μF, R_L = 100Ω. See Figure 1.				3	ms
Turn-Off Time	t_{OFF}	C_L = 1μF, R_L = 100Ω. See Figure 1.				1	ms
Output Discharge							
Discharge Resistance[6]	R_{DIS}	VIN= 5V, Disabled, I_{OUT} =1mA			600		Ω
Fault Flag							
FAULT Output Low Voltage	V_{OL}	I_{FAULT} = 1mA				180	mV
FAULT Off Current	I_{FOH}	V_{FAULT} = 6V				1	uA
FAULT Blanking and Latch Off Time(Over-Current)	t_{Blank_OC}	Assertion or de-assertion due to overcurrent		5	7.5	10	ms
Thermal Shutdown							
Thermal Shutdown Threshold[7]	T_{SHDN}	Enabled, R_{LOAD} = 1kΩ			160		℃
Thermal Shutdown Threshold under Current Limit[7]	T_{SHDN_OCP}	Enabled, R_{LOAD} = 1kΩ			140		℃
Thermal Shutdown Hysteresis[7]	T_{HYS}				20		℃

Table 18: Electrical Characteristics

9. CI INTERFACE

17MB185Y Digital CI and Smart Card Interface Block diagram:

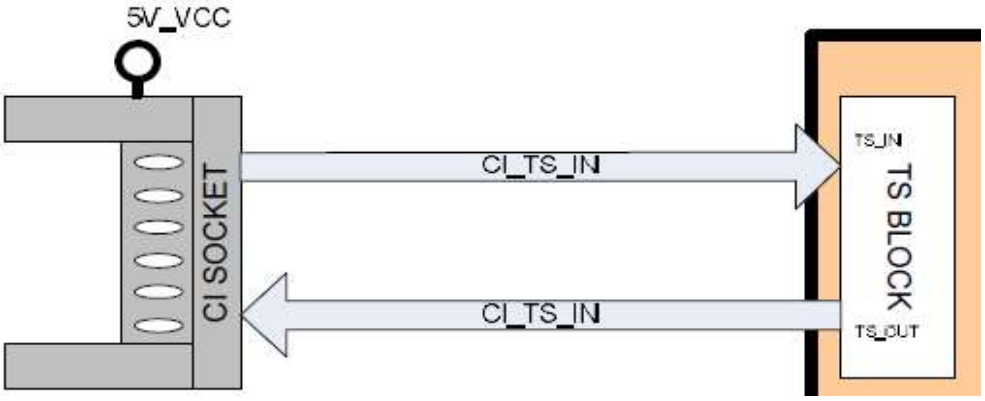


Figure 22: CI Interface

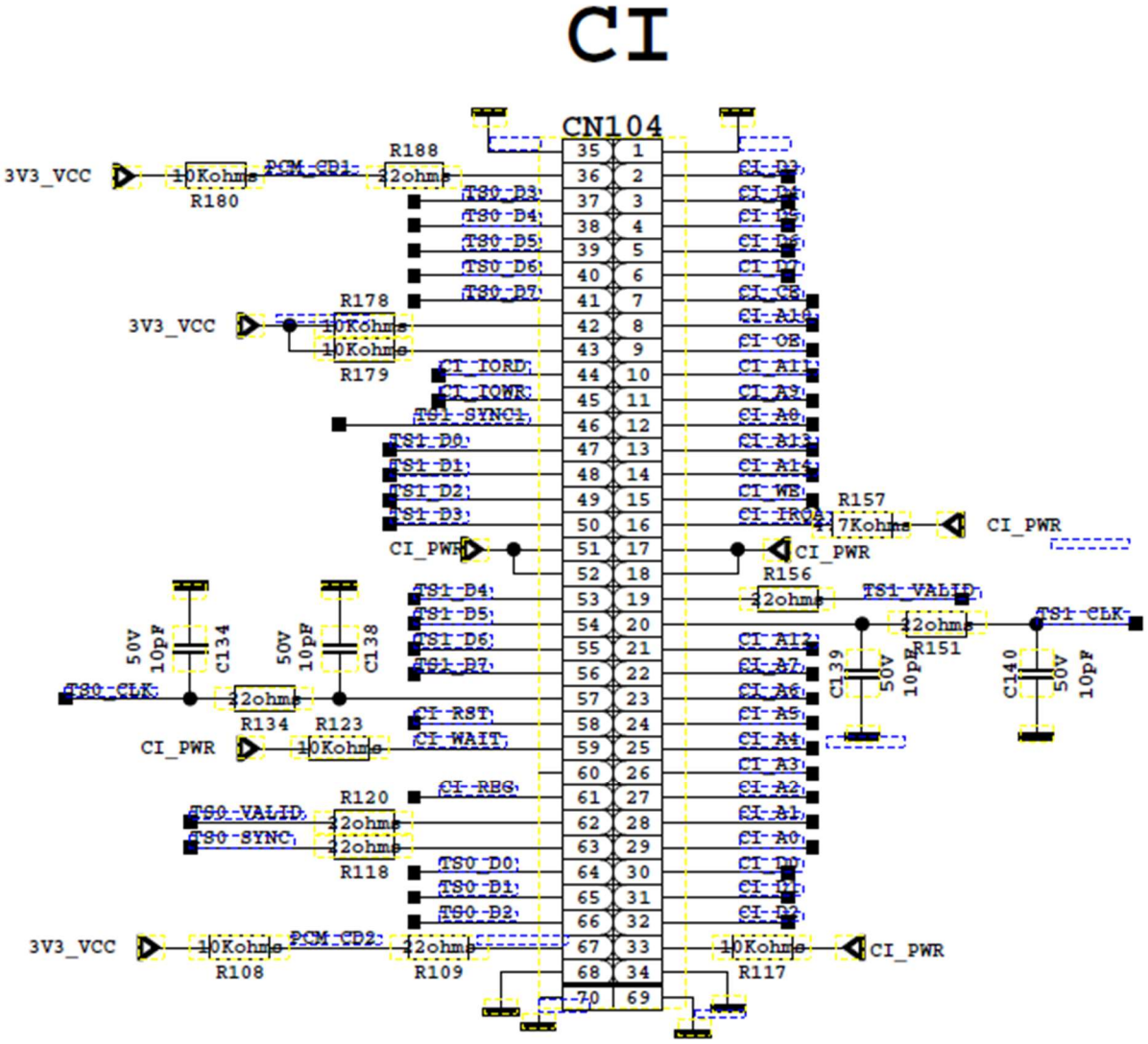


Figure 23: CI Schematic

10. SOFTWARE UPDATE

MAIN SOFTWARE UPDATE

In 17MB185Y project, please follow software update procedure:

Method-1

1. Copy MstarUpgrade.bin to USB stick (root directory, FAT32)
2. Enter M-Boot console first (Long press "ENTER" key on Tera Term Console when your device reboot then do AC On)
3. Plug the USB stick to your target board
4. Execute "custar" in M-Boot console to perform upgrading

Method-2

1. Copy upgrade_loader.pkg to root folder of USB stick (or copy Upgrade_loader_no_tvcertificate.pkg if you don't want to erase keys, credentials, etc.)
2. Insert USB disk to one of the USB ports on your TV
3. Power on TV and wait until you see the boot logo

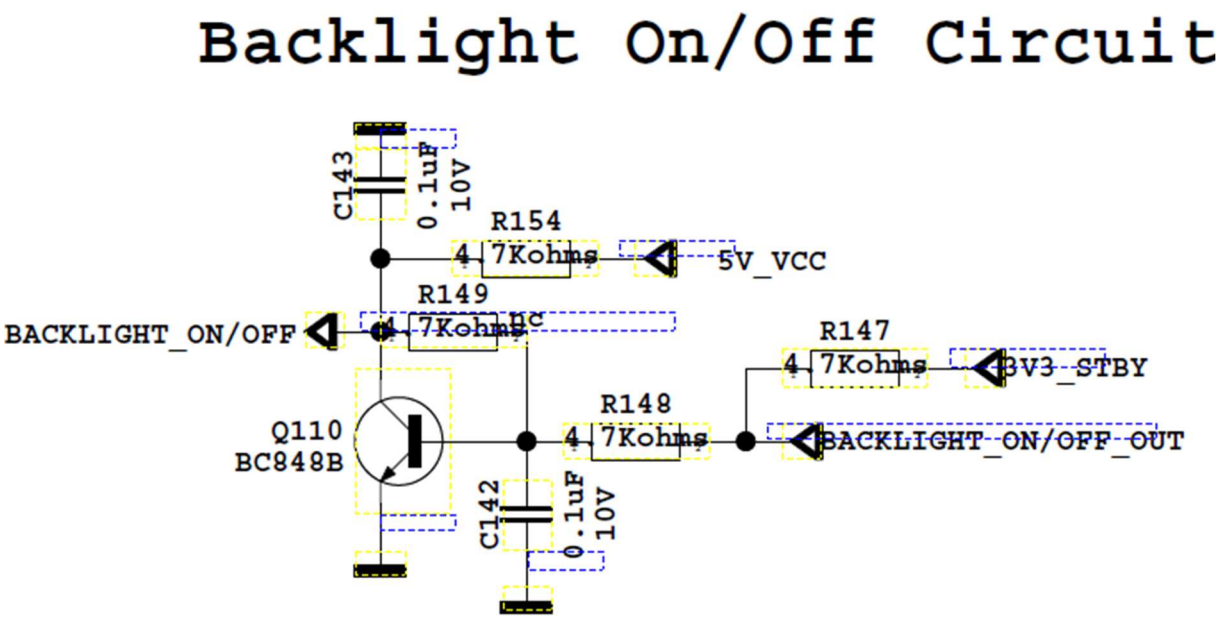
11. TROUBLESHOOTING

A. NO BACKLIGHT PROBLEM

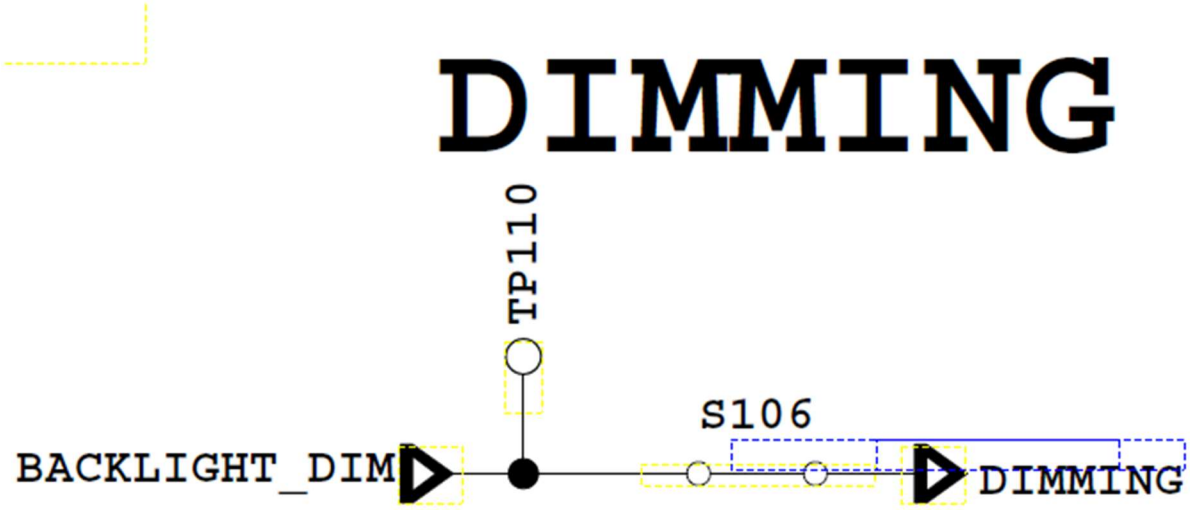
Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible causes: Backlight pin, dimming pin, backlight supply, stby on/off pin

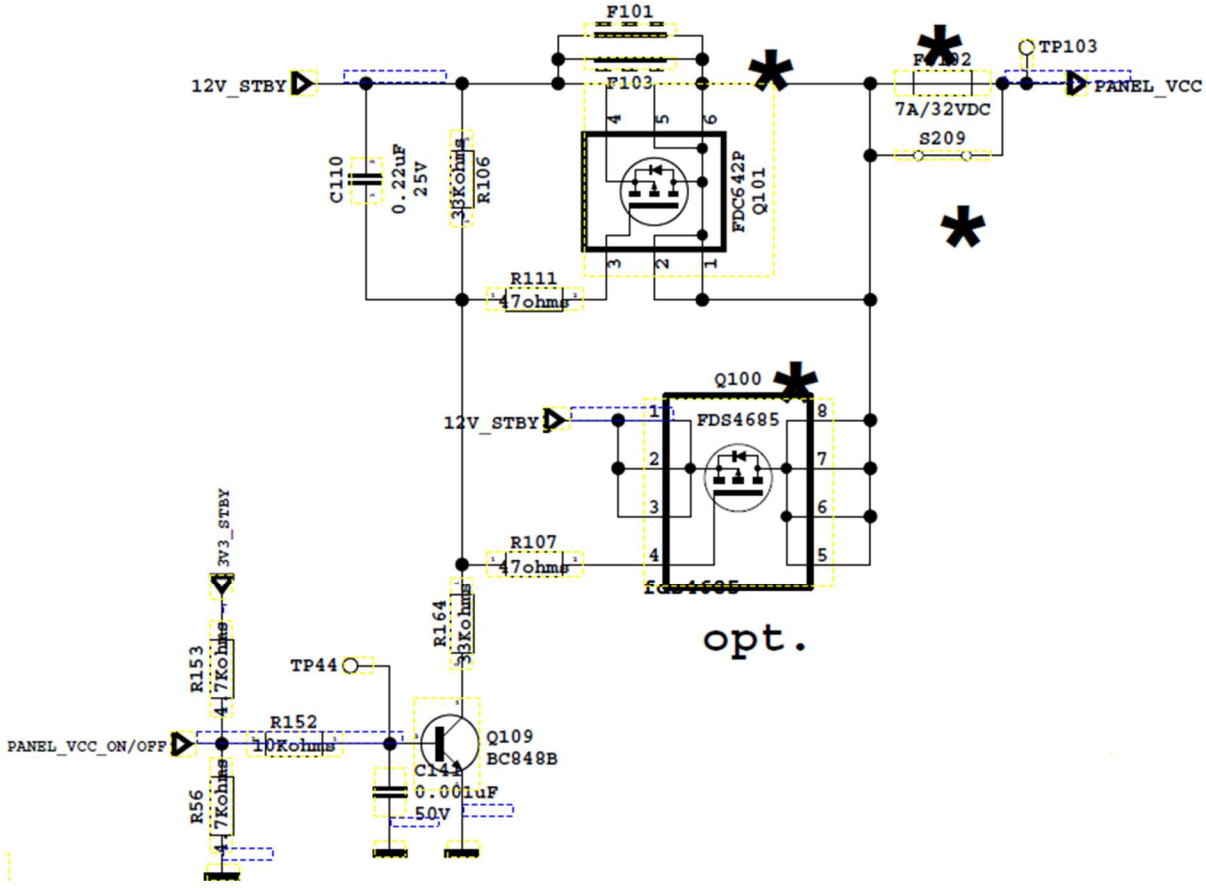
BACKLIGHT_ON/OFF pin should be high when the backlight is ON. Collector pin of Q110 must be low when the backlight is OFF. Please also check panel cables.



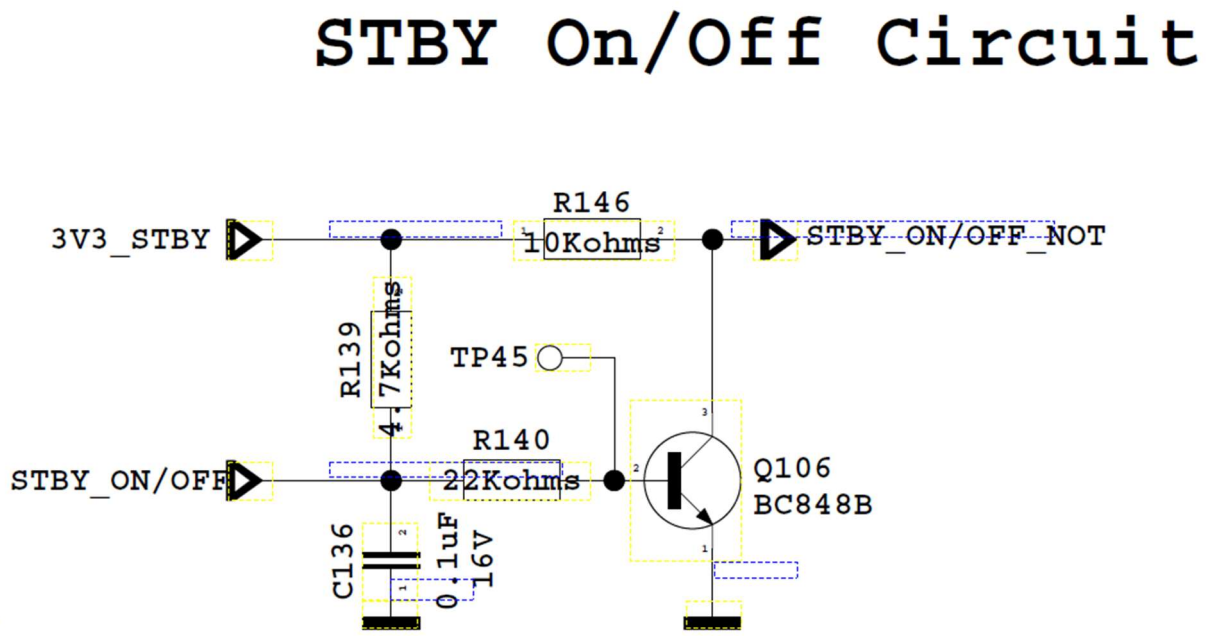
Dimming pin should be high or square wave in open position. It also can be checked at TP110. Please also check panel or power cables and connectors.



Backlight power supply should be in panel specs. Please check Q101, shown below; also it can be checked TP103.



STBY_ON/OFF_NOT should be low for TV on condition, please check Q106's collector.

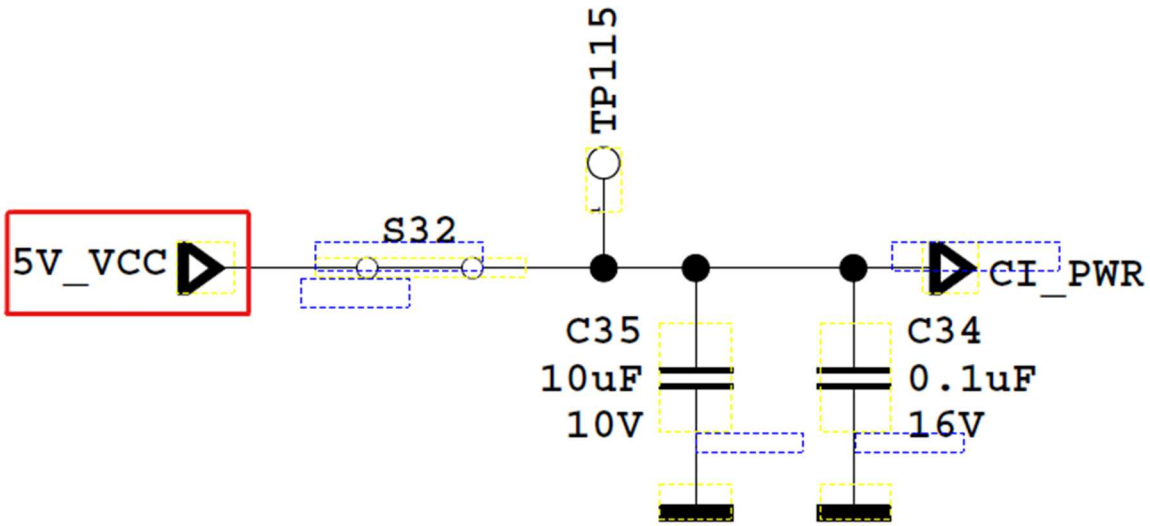


B. CI MODULE PROBLEM

Problem: CI is not working when CI module inserted.

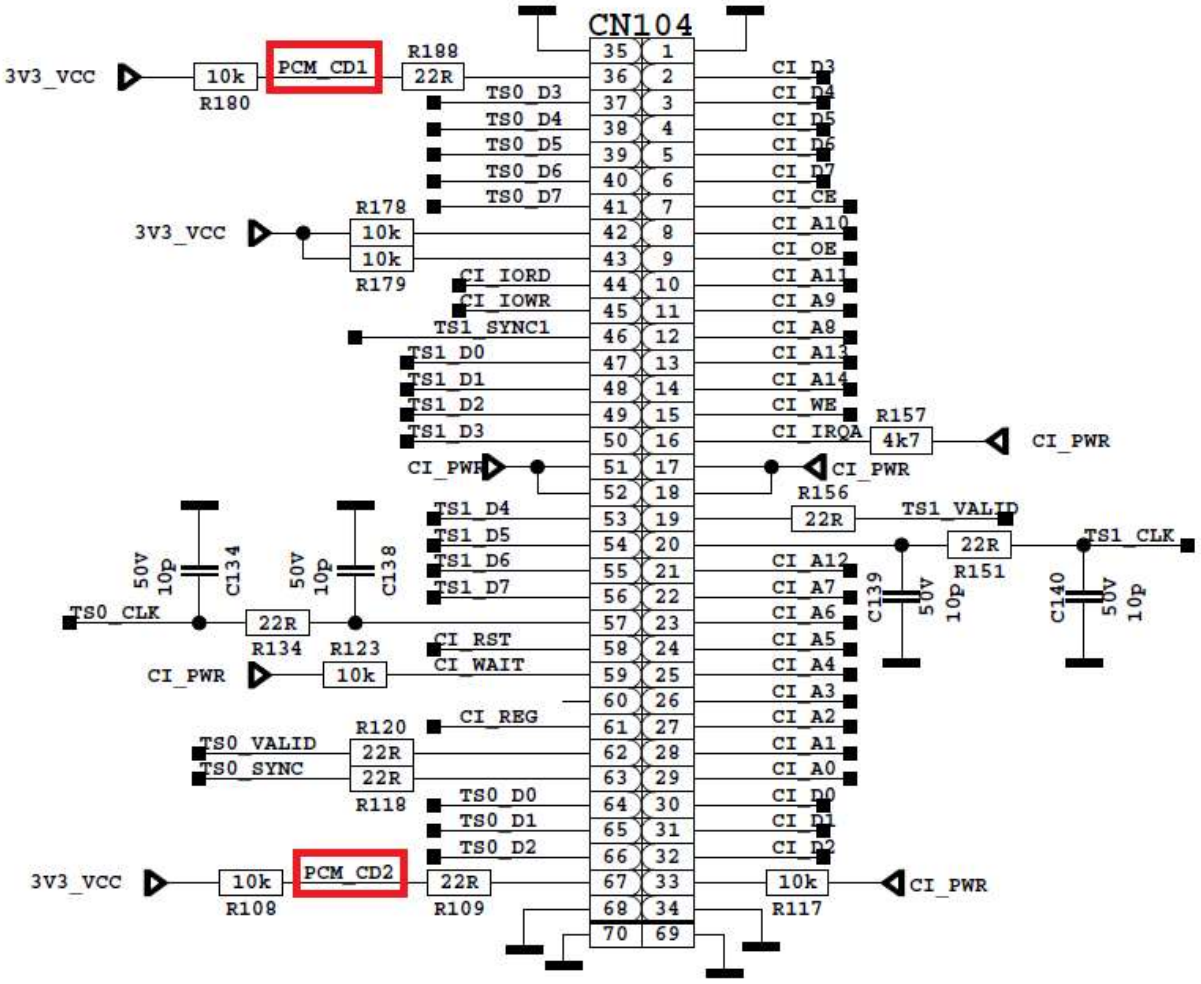
Possible causes: Supply, supply control pin, detects pins, mechanical positions of pins.

- CI supply should be 5V when CI module inserted. If it is not 5V please check CI_PWR_CTL, this pin should be low.



- Please check mechanical position of CI module. Is it inserted properly or not?
- Detect ports should be low. If it is not low please check CI connector pins, CI module pins.

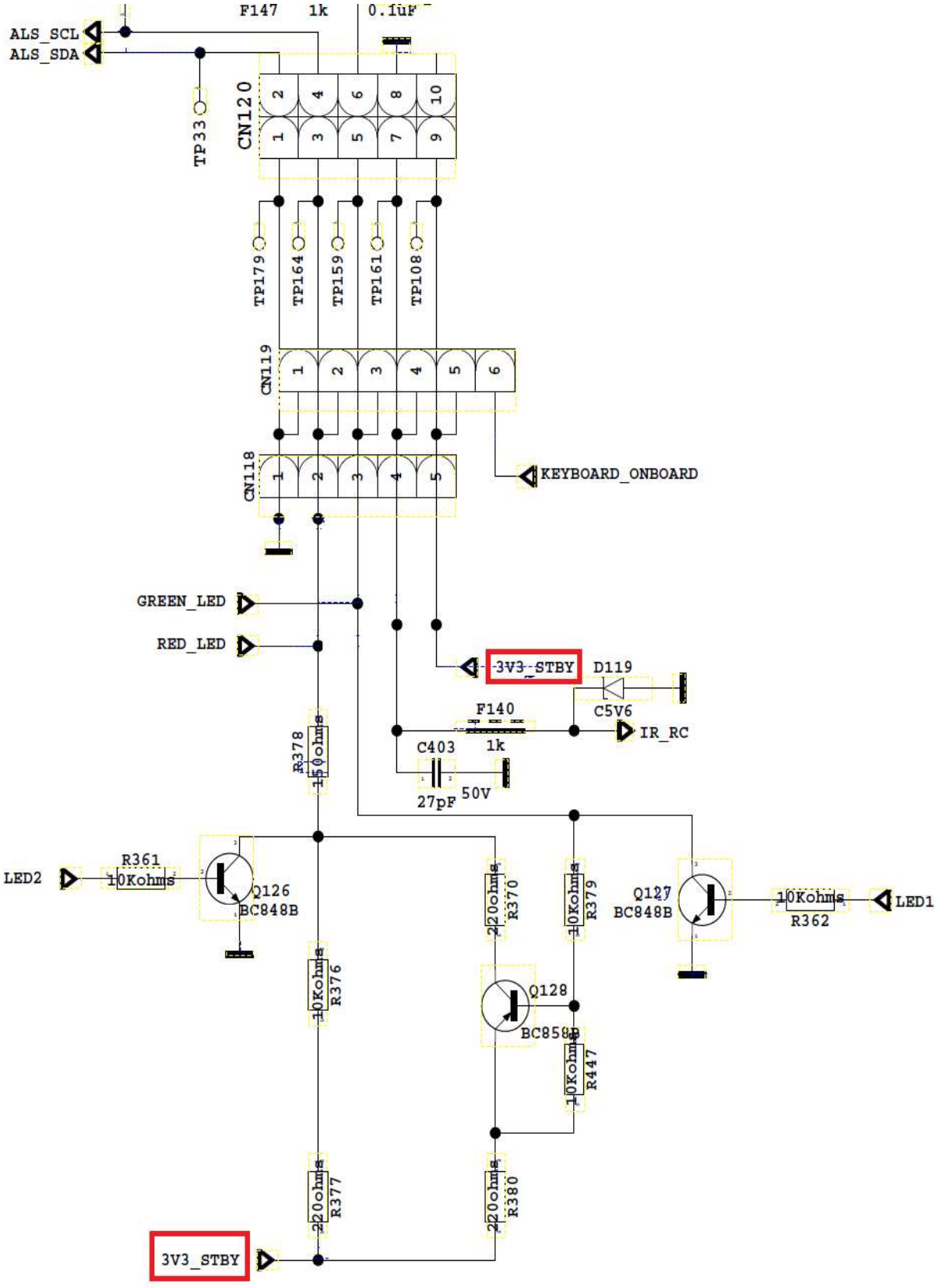
CI


CN104
3V3_VCC
10k
R180
PCM_CD1
R188
22R
TS0_D3
TS0_D4
TS0_D5
TS0_D6
TS0_D7
R178
10k
10k
R179
CI_IORD
CI_IOWR
TS1_SYNC1
TS1_D0
TS1_D1
TS1_D2
TS1_D3
CI_PWR
TS1_D4
TS1_D5
TS1_D6
TS1_D7
50V
10p
C134
C138
TS0_CLK
22R
R134
R123
10k
CI_RST
CI_WAIT
CI_REG
R120
TS0_VALID
TS0_SYNC
22R
22R
R118
TS0_D0
TS0_D1
TS0_D2
PCM_CD2
R108
R109
CI_D3
CI_D4
CI_D5
CI_D6
CI_D7
CI_CE
CI_A10
CI_OE
CI_A11
CI_A9
CI_A8
CI_A13
CI_A14
CI_WE
CI_IRQA
R157
4k7
CI_PWR
CI_PWR
R156
22R
TS1_VALID
22R
R151
TS1_CLK
CI_A12
CI_A7
CI_A6
CI_A5
CI_A4
CI_A3
CI_A2
CI_A1
CI_A0
CI_D0
CI_D1
CI_D2
10k
R117
CI_PWR

C. IR PROBLEM

Problem: LED or IR not working

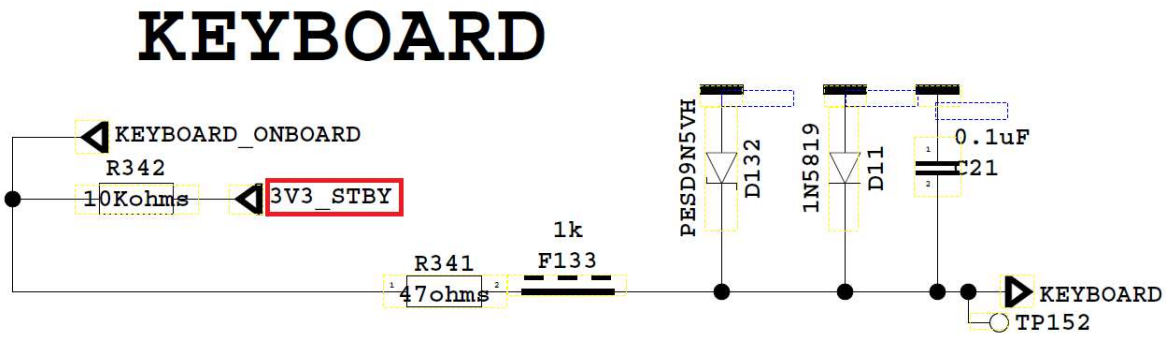
Check LED card supply on 17MB185Y chasis.



D. KEYPAD TOUCHPAD PROBLEMS

Problem: Keypad or Touchpad is not working

Check keypad supply on 17MB185Y.

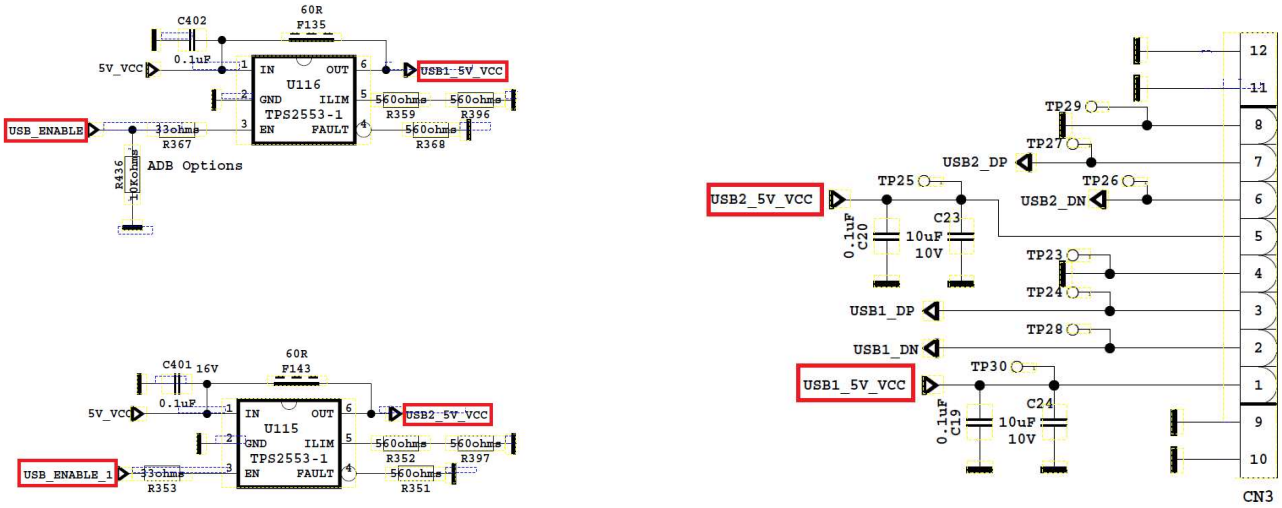


E. USB PROBLEMS

Problem: USB is not working or no USB Detection.

Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.

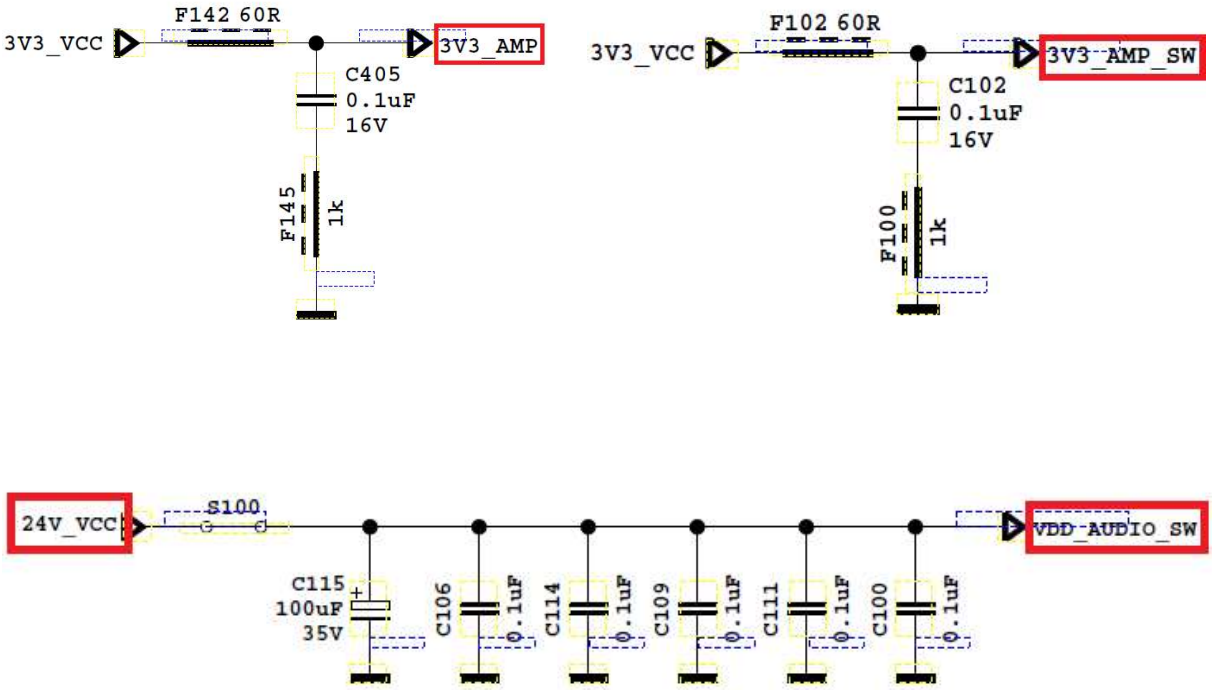
USB Control is optional, so U115 and U116 may not be added. Check supply voltages only.



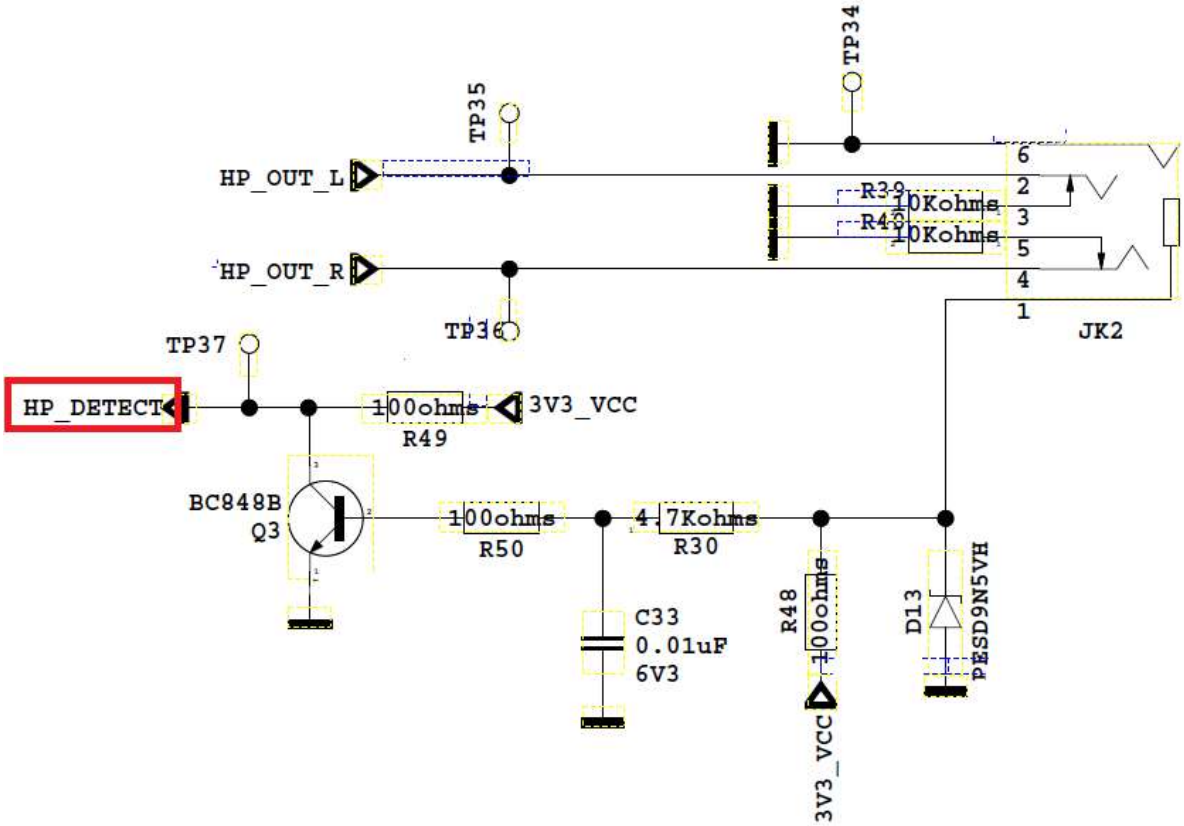
F. NO SOUND PROBLEM

Problem: No audio at main TV speaker outputs.

Check supply voltages of 24V_VCC, VDD_AUDIO and 3V3_AMP with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3V.



HEADPHONE OUTPUT



G. STANDBY ON/OFF PROBLEM

Problem: Device cannot boot, TV hangs in standby mode.

There may be a problem about power supply. Check main supplies with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via Teraterm program. These printouts may give a clue about the problem. You can use VGA for Teraterm program connection.

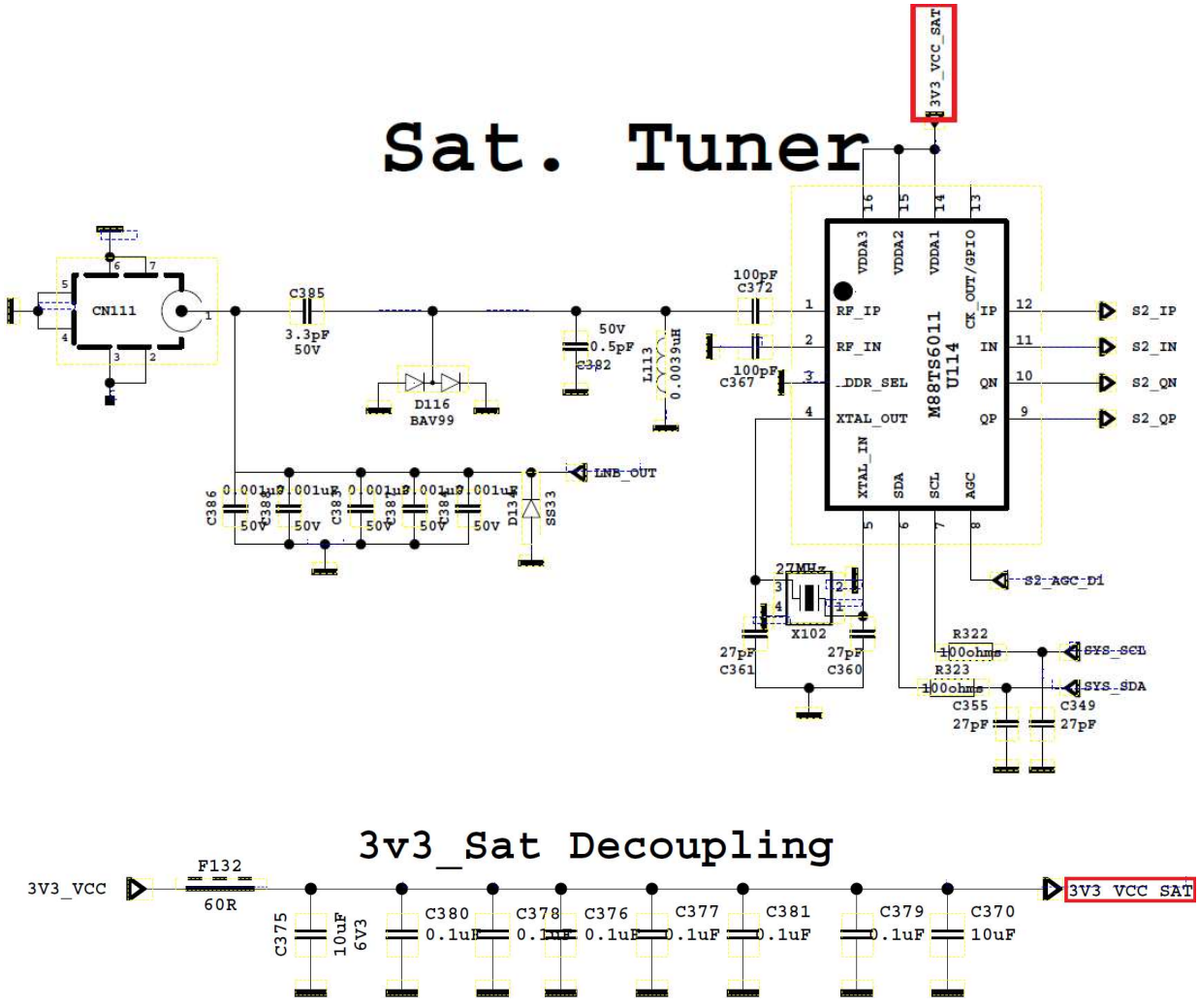
H. NO SIGNAL PROBLEM IN DVB-S/S2 MODE

Problem: No signal or Low signal in DVB-S/S2 mode.

Check signal cables and LNB voltage, if there is no problem, check M88TS6011 (U114) supply voltages; 3V3_VCC_SAT.

If the above measurements are OK, then measure the voltage from the PIN1 of U114.

If the PIN9 voltage is equal to 0V, please check i2c waveforms and software. If the PIN9 voltage is lower than 1V (e.g: 0.8V or 0.3V), change the U114 with a new part.

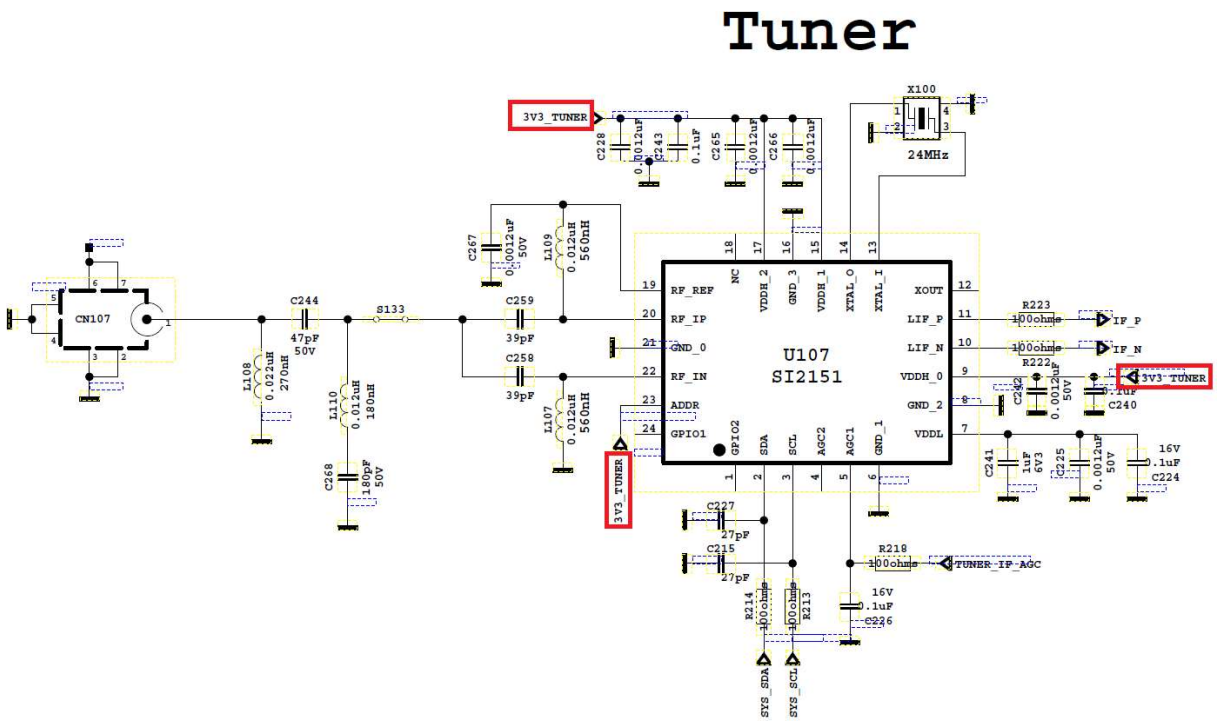


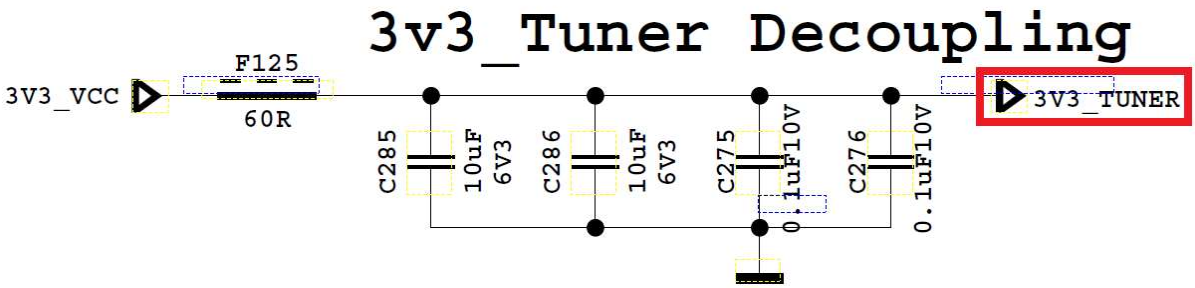
İ. *NO SIGNAL PROBLEM IN DVB-T MODE*

Problem: No signal or Low signal in DVB-T mode.

Check signal cables and LNB voltage, if there is no problem, check SI2151 (U107) supply voltages; 3V3_TUNER.

If the above measurements are OK, then change the U107 with a new part.

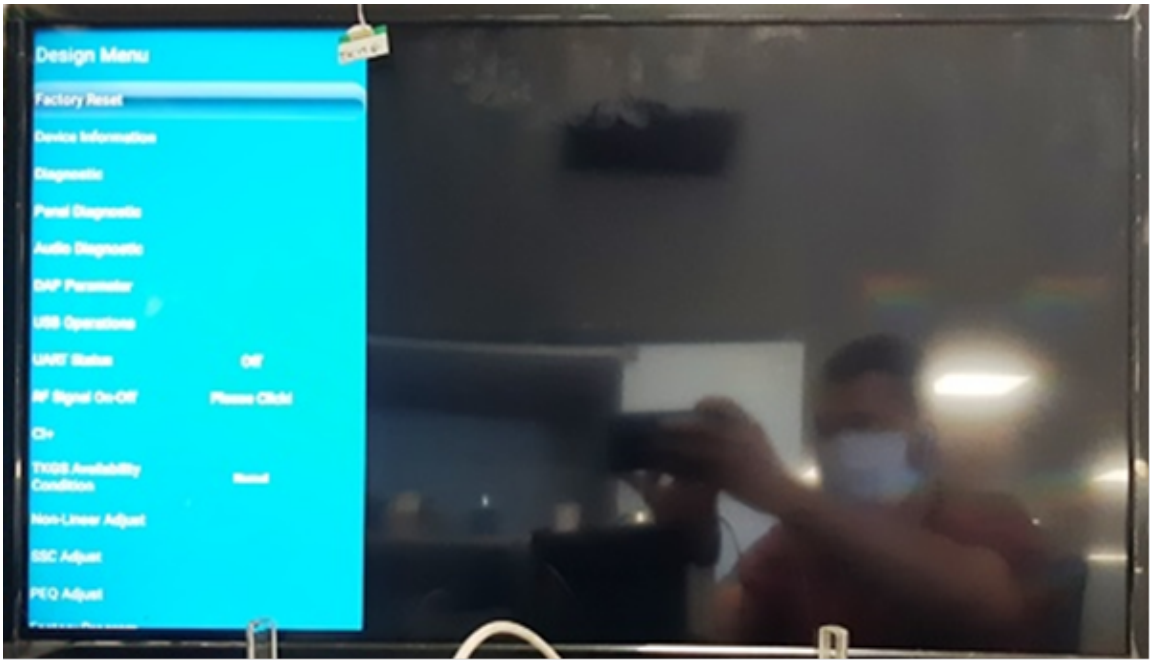




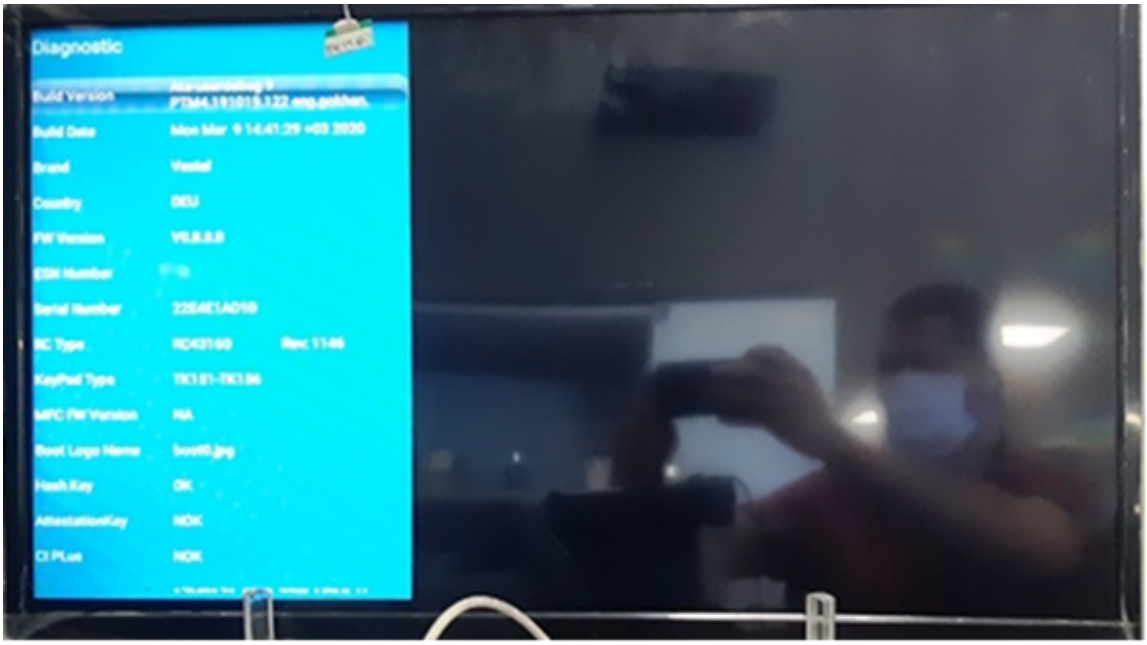
12. SERVICE MENU SETTINGS

In order to reach service menu, first chose Channel, then press **“MENU”** button, press **“Advanced Options”** then write “**4725”** by using remote controller.

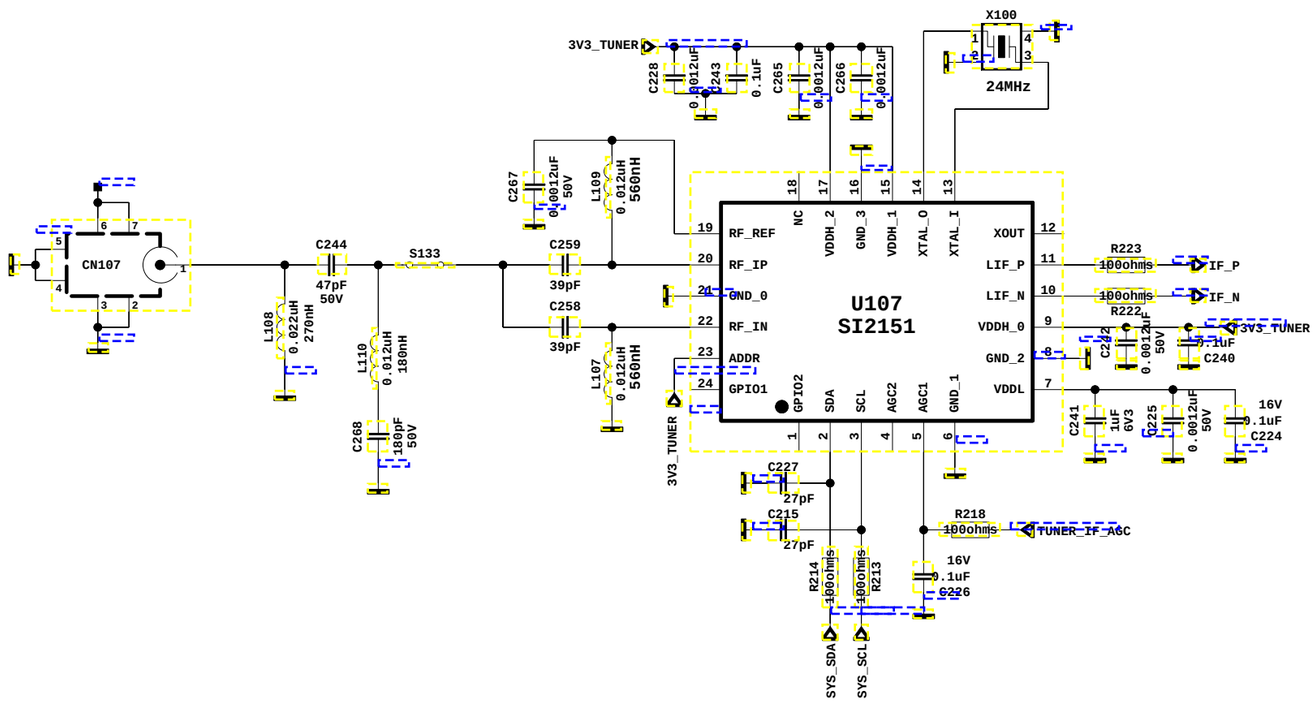
You can see the service menu main screen below. You can check SW releases by using this menu under Diagnostic title. In addition, you can make changes on video settings, audio settings, DAP Parameters etc. using regarding titles. You may also use USB Operations for SW update and update Unique Keys and Configuration files.



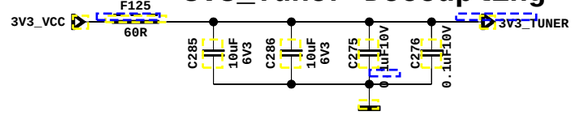
Service Menu



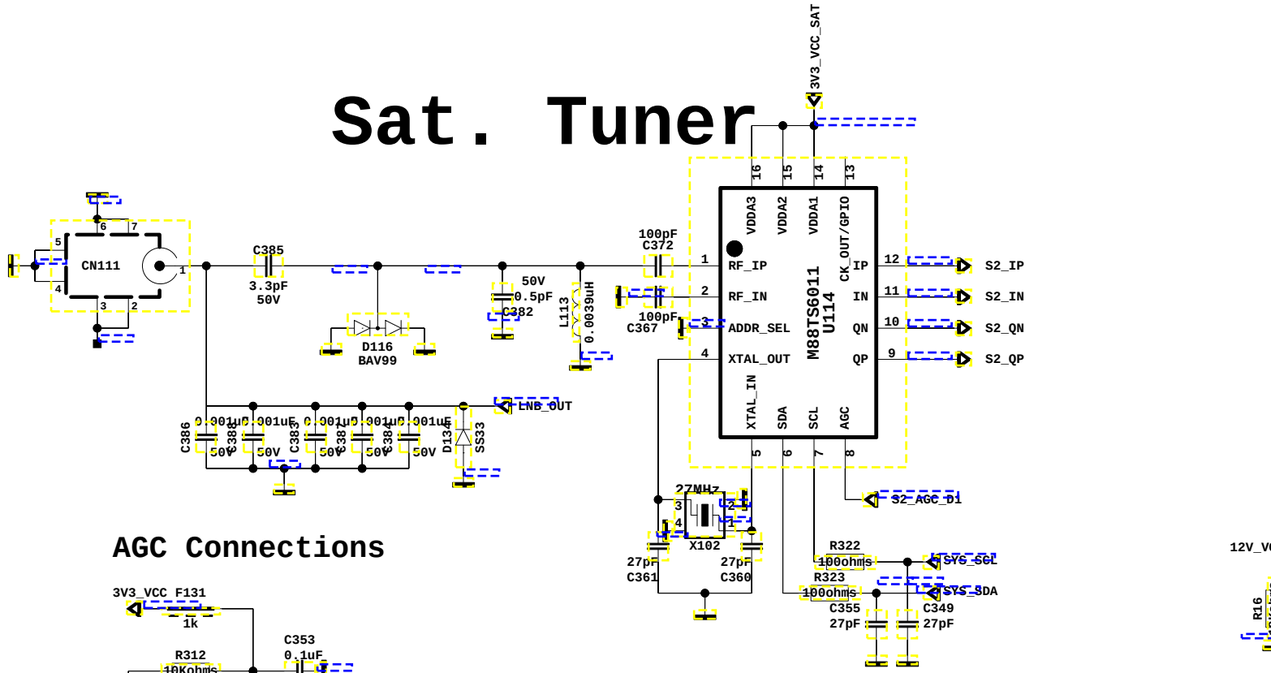
Tuner



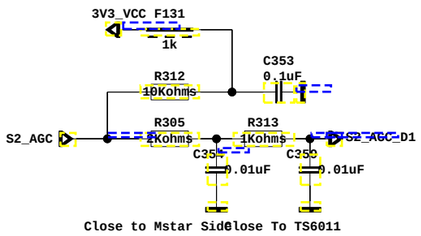
3v3_Tuner Decoupling



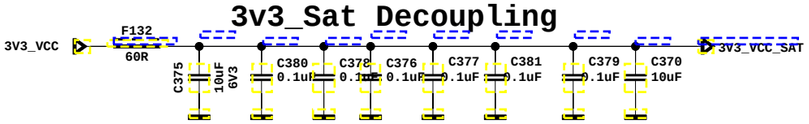
Sat. Tuner



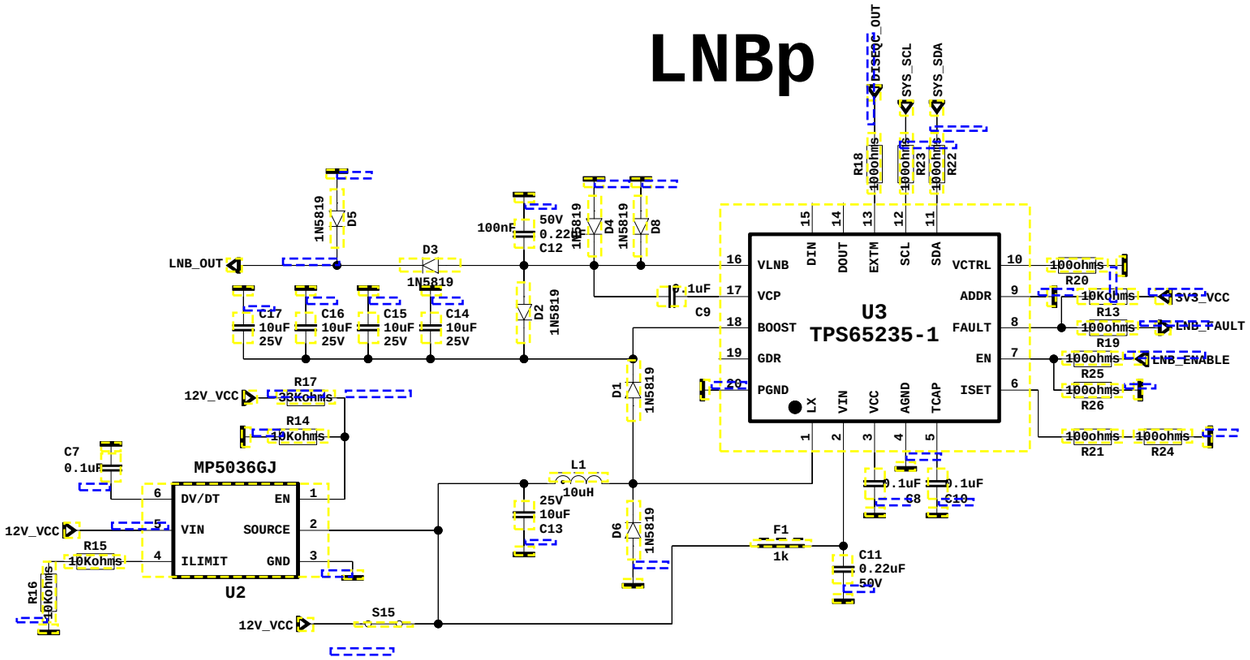
AGC Connections



3v3_Sat Decoupling



LNBp



VESTEL	PROJECT NAME : 17mb185y-r1a	A3
SCH NAME :TUNER_SAT_LNB		T. SHT 8
DRAWN BY :<YOUR NAME HERE>		24/05/2022:09:35

TCONLESS/VBYONE SOCKET

CN106 (70-69) — PMIC_GPIO, PAN_SDA, PAN_SCL, VES12N, VES12P, VES11N, VES11P, VES10N, VES10P, VES9N, VES9P, VES8N, VES8P, VES7N, VES7P, VES6N, VES6P, VES5N, VES5P, VES4N, VES4P, VES3N, VES3P, VES2N, VES2P, VES1N, VES1P, LOCKN, DEMURA_CS, DEMURA_DI, DEMURA_DO, DEMURA_CLK, TCON1/GST, TCON5/MCLK, TCON6/GCLK, TCON7/EO, TCON2, TCON3, TCON0, TCON4, 3V3_VCC, DEMURA_WP

CN105 (53-52) — OP_PIN38, OP_PIN37, OP_PIN36, OP_PIN35, OP_PIN34, OP_PIN33, OP_PIN32, OP_PIN31, OP_PIN30, OP_PIN29, OP_PIN28, VBY_HTPDN, VBY_LOCKN, VBY_0N, VBY_0P, VBY_1N, VBY_1P, VBY_2N, VBY_2P, VBY_3N, VBY_3P, VBY_4N, VBY_4P, VBY_5N, VBY_5P, VBY_6N, VBY_6P, VBY_7N, VBY_7P

F124, F121, F119 — PANEL_VCC

VES12N C177 0.1uF VBY_0N
VES12P C174 0.1uF VBY_0P
VES11N C173 0.1uF VBY_1N
VES11P C175 0.1uF VBY_1P
VES10N C171 0.1uF VBY_2N
VES10P C172 0.1uF VBY_2P
VES9N C170 0.1uF VBY_3N
VES9P C169 0.1uF VBY_3P
VES8N C167 0.1uF VBY_4N
VES8P C168 0.1uF VBY_4P
VES7N C165 0.1uF VBY_5N
VES7P C166 0.1uF VBY_5P
VES6N C161 0.1uF VBY_6N
VES6P C162 0.1uF VBY_6P
VES5N C160 0.1uF VBY_7N
VES5P C156 0.1uF VBY_7P

VES_LOCKN — F116 1k — TP43 — VBY_LOCKN
TCON5/MCLK — F117 1k — TP133 — VBY_HTPDN

TCON_SCL — S134 — PAN_SCL
TCON_SDA — S135 — PAN_SDA

PANEL_VCC — S128 — OP_PIN38
PAN_SCL — S126 — S127
PANEL_VCC — R217 38Kohms — R212 10Kohms — OP_PIN37
PANEL_VCC — R216 38Kohms — R211 10Kohms — OP_PIN36
PAN_SDA — S130 — S129
PANEL_VCC — R215 38Kohms — R210 10Kohms — OP_PIN35
PAN_SDA — S131 — OP_PIN34
PAN_SCL — S132 — OP_PIN33
PANEL_VCC — R220 38Kohms — R221 10Kohms — OP_PIN32
PANEL_VCC — R207 38Kohms — R208 10Kohms — OP_PIN31
PANEL_VCC — R206 38Kohms — R209 10Kohms — OP_PIN30
PANEL_VCC — S123 — S124 — OP_PIN29
PANEL_VCC — R205 38Kohms — S125 — OP_PIN28

12V_STBY — F101 — F103 — FDC642P Q101 — FS102 7A/32VDC — TP103 — PANEL_VCC
C110 0.22uF 25V — 33Kohms R106
R111 47ohms
12V_STBY — Q100 FDS4685 — R107 47ohms — fds4435
R164 33Kohms — TP44 — Q109 BC848B — C141 0.001uF 50V
PANEL_VCC_ON/OFF — R152 10Kohms — R153 4.7Kohms — 3V3_STBY
R56 4.7Kohms

* JUST ONE OF THEM SHOULD BE USED

opt.

12V_VCC — R273 10Kohms — R274 1Kohms — POWER_SENSE
needs GND shielding
R275 1Kohms — D109 C3V6 — C325 3300uF

BACKLIGHT_ON/OFF_OUT — AH3
MIC_MUTE — N2
S2
AMP_MUTE — R2
AC4
S1
LED2 — M2
GPIO2_PM — M1
GPIO9_PM — Y3
GPIO10_PM
3V3_STBY — R248 1Kohms — C298 0.1uF 16V — C299 0.1uF 10V — D108 1N4148 — R247 10Kohms — C295 0.1uF 10V
STBY_ON/OFF — P2
LED1 — V5
H6
3V3_STBY — 4.7Kohms — TP191 — R244
DEBUG_RX — B20
DEBUG_TX — A20
3V3_STBY — 4.7Kohms — TP192 — R241
KEYBOARD — J4
J5
3V3_STBY — 4.7Kohms — AC5
PANEL_VCC_ON/OFF — Y8
WOWL_DET — AC9
POWER_SENSE — AB9
H5
D123 RESD9N5VH
3V3_STBY — 4.7Kohms — R382
CORE_VID0 — U5
CPU_VID1 — P7
CPU_VID2 — P3
LD_SPI_MISO — R53 100ohms — R55
LD_SPI_CS — 100ohms
LD_SPI_MOSI — R52 100ohms — R54
LD_SPI_CK — 100ohms
DEMURA_DO — 4.7Kohms — E14
R385
DEMURA_DI — 4.7Kohms — D17
DEMURA_CLK — 4.7Kohms — R387 — E17
R388 — D14
C157 50V 10pF — DEMURA_CS — E18
GPIO0

SAR0
SAR1
SAR2
SAR3
VPLUGIN
VID0
VID1
VID2
LD_SPI_MISO_/_SPI2_DI
LD_SPI_CS_/_SPI2_CK
LD_SPI_MOSI_/_SPI1_DI
LD_SPI_CK_/_SPI1_CK

U108
MT9685LAAJAC

LVSYNC_/_Mini_A_5-_/_VX1_0-
LHSYNC_/_Mini_A_5+_/_VX1_0+
LDE_/_Mini_A_4-_/_VX1_1-
LCK_/_Mini_A_4+_/_VX1_1+
LVB0-_/_Mini_A_3-_/_VX1_2-
LVB0+_/_Mini_A_3+_/_VX1_2+
LVB1-_/_Mini_A_CK-_/_VX1_3-
LVB1+_/_Mini_A_CK+_/_VX1_3+
LVB2-_/_Mini_A_2-_/_VX1_4-
LVB2+_/_Mini_A_2+_/_VX1_4+
LVBCLK-_/_Mini_A_1-_/_VX1_5-
LVBCLK+_/_Mini_A_1+_/_VX1_5+
LVB3-_/_Mini_A_0-_/_VX1_6-
LVB3+_/_Mini_A_0+_/_VX1_6+
LVB4-_/_Mini_B_5-_/_VX1_7-
LVB4+_/_Mini_B_5+_/_VX1_7+
LVA0-_/_Mini_B_4-_/_Vx1_OSD_00-
LVA0+_/_Mini_B_4+_/_Vx1_OSD_00+
LVA1-_/_Mini_B_3-Vx1_OSD_01-
LVA1+_/_Mini_B_3+_/_Vx1_OSD_01+
LVA2-_/_Mini_B_CK-_/_Vx1_OSD_02-
LVA2+_/_Mini_B_CK+_/_Vx1_OSD_02+
LVACLK-_/_Mini_B_2-_/_Vx1_OSD_03-
LVACLK+_/_Mini_B_2+_/_Vx1_OSD_03+
LVA3-_/_Mini_B_1-_/_LOCKN
LVA3+_/_Mini_B_1+_/_HTPDN
LVA4-_/_Mini_B_0-_/_OSD_LOCKn
LVA4+_/_Mini_B_0+_/_OSD_HTPDn

4

C1 VES12N
C2 VES12P
B1 VES11N
B2 VES11P
B3 VES10N
A3 VES10P
C3 VES9N
B4 VES9P
C4 VES8N
B5 VES8P
A5 VES7N
C5 VES7P
A6 VES6N
B6 VES6P
C6 VES5N
B7 VES5P
B8 VES4N
C8 VES4P
B9 VES3N
A9 VES3P
C9 VES2N
A10 VES2P
B10 VES1N
C10 VES1P
B11 VES_LOCKN
C11 TCON5/MCLK
B12 10Kohms — 3V3_VCC — R183
C12 10Kohms — 3V3_VCC — R185
S117 — TCON6/GCLK
S118 — TCON7/EO

Mini_C_5- F4
Mini_C_5+ F3
Mini_C_4- F5
Mini_C_4+ F6
Mini_C_3- E2
Mini_C_3+ E3
Mini_C_CK- D2
Mini_C_CK+ D1
Mini_C_2- E5
Mini_C_2+ E4
Mini_C_1- D4
Mini_C_1+ D5
Mini_C_0- D6
Mini_C_0+ D7
Mini_D_5- E7
Mini_D_5+ F7
Mini_D_4- E8
Mini_D_4+ F8
Mini_D_3- D8
Mini_D_3+ D9
Mini_D_CK- D10
Mini_D_CK+ E10
Mini_D_2- F11
Mini_D_2+ E11
Mini_D_1- D11
Mini_D_1+ D12
Mini_D_0- E12
Mini_D_0+ F12

R1 4.7Kohms — 3V3_STBY
BT_WAKE — U2 — GPIO7_PM
USB_ENABLE_1 — AB4 — GPIO8_PM
WOWL_EN — H3 — GPIO11_PM
WIFI_RST — M4 — GPIO12_PM
3V3_STBY — 4.7Kohms — R432

LNB_FAULT — AD10 — GPIO9
LNB_ENABLE — AC16 — GPIO10

R5 4.7Kohms — R7 4.7Kohms — R8 4.7Kohms — R9 4.7Kohms

TCON0 C13 S115 — TCON0
TCON1 A14 S116 — TCON1/GST
TCON2 B14 S113 — TCON2
TCON3 C14 S110 — TCON3
TCON4 B15 S114 — TCON4

GPIO11 M3 — AMP_RST
GPIO12 L3 — HP_DETECT
R393 10Kohms — 3V3_VCC

PWM0 A19 — BACKLIGHT_DIM
PWM1 C17 — VSYNC_LIKE
PWM2 C19 — IR_LED

TESTPIN D18

1V8 TCON Level Shifter

S119 — Q112 — VES_LOCKN — LOCKN
PANEL_VCC — R181 10Kohms — 10Kohms R187
R182 10Kohms

CHIP CONFIGURATION

CHIP_CONFIG[2:0]={PAD_PM_GPIO9,PAD_PM_GPIO10,PAD_PM_GPIO2}

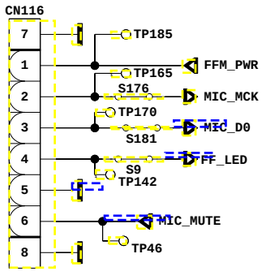
3V3_STBY — R246 4.7Kohms — nc — GPIO9_PM — R245 4.7Kohms
3V3_STBY — R260 4.7Kohms — GPIO10_PM — R256 4.7Kohms — nc
3V3_STBY — R272 4.7Kohms — nc — GPIO2_PM — R271 4.7Kohms — GPIO2_PM

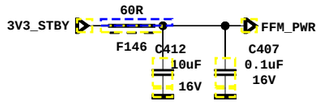
CN101 — 75LG_VCC — PANEL_VCC — C103 1uF 10V — C104 0.1uF 10V

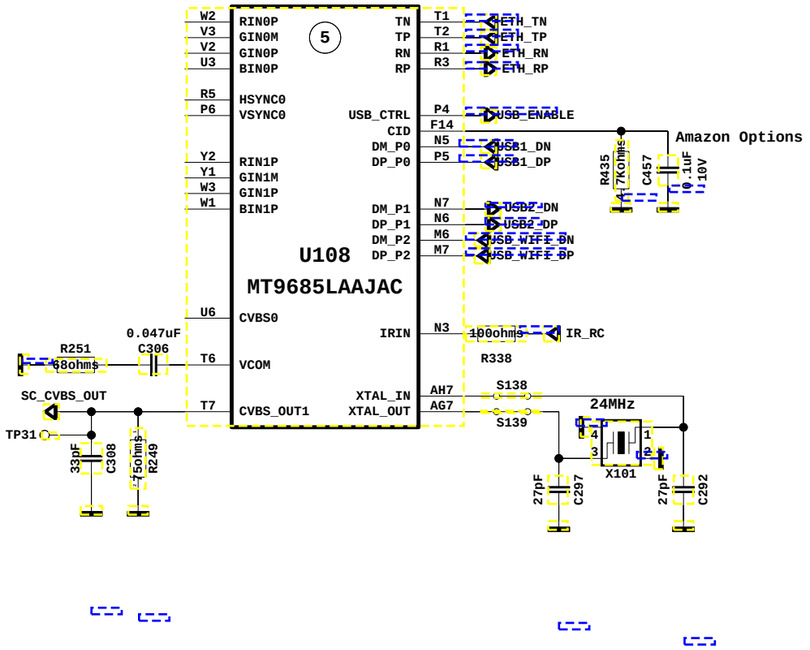
Value	Description
3'b010	ARM boot from ROM; outer storage is eMMC
3'b011	ARM boot from ROM; outer storage is NAND

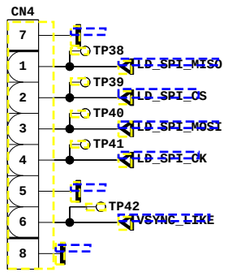
VESTEL | PROJECT NAME : 17mb185y-r1a | A3
SCH NAME :VBYONE | T. SHT 8
DRAWN BY :<YOUR NAME HERE> | 24/05/2022:09:33

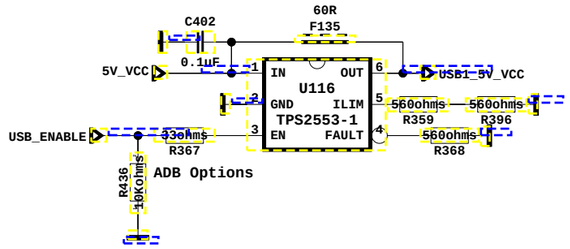
FFGA INTERFACE



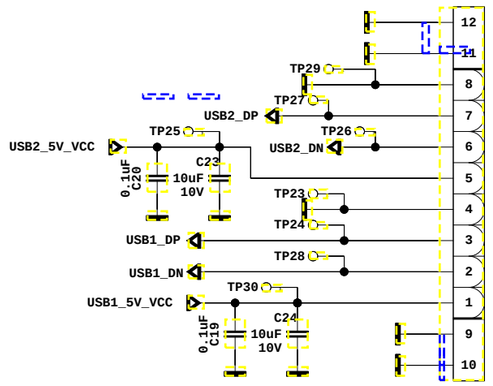




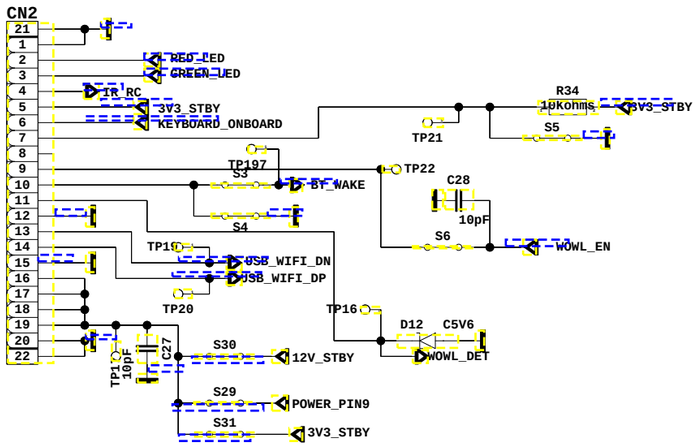


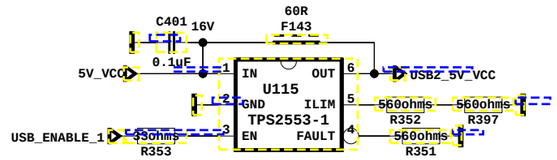


USB1&2 2.0



WIFI&BT&LED_IR

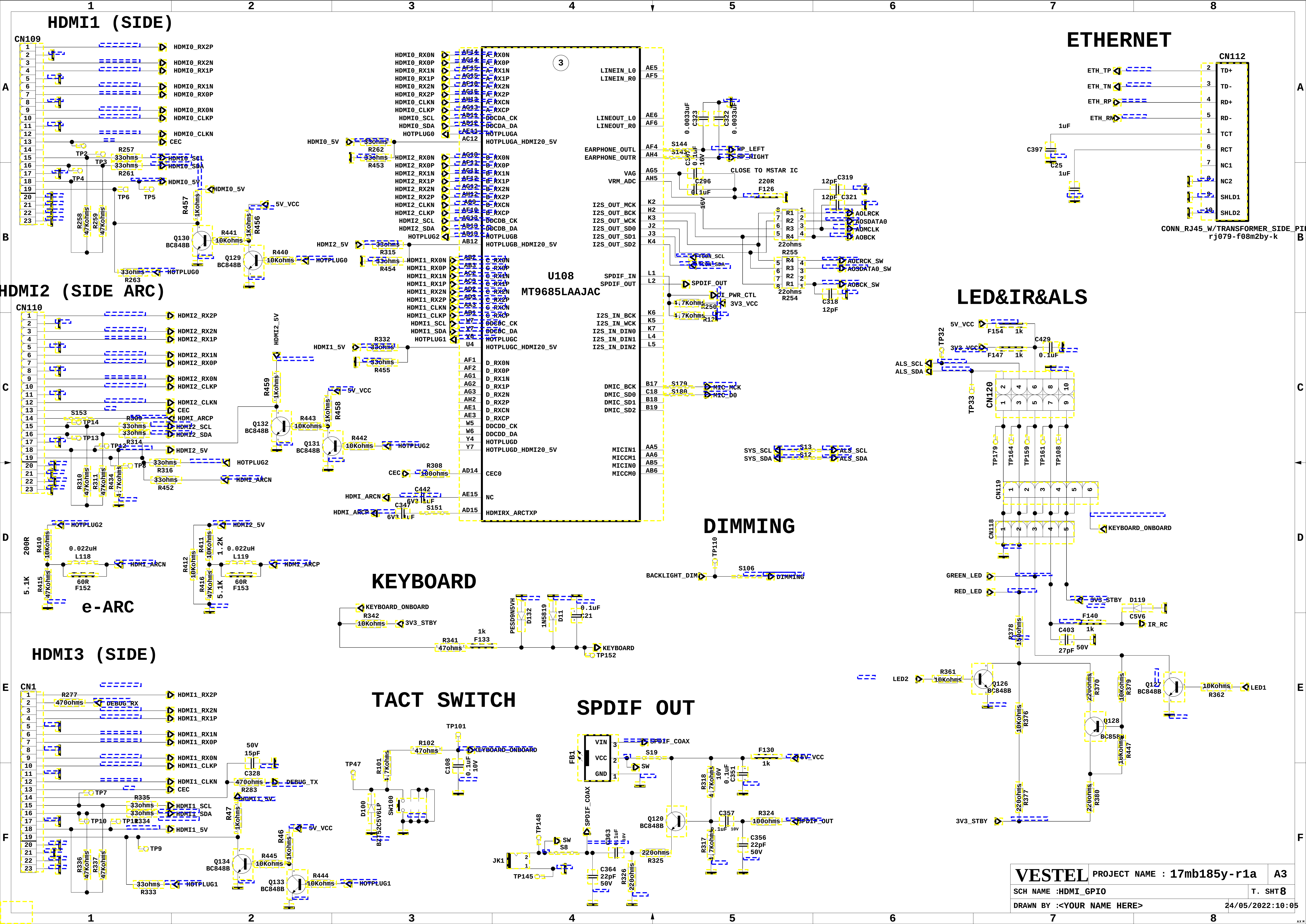




TEK USB OPSIYONU ICIN KONNEKTOR

TEK USB OPSIYONU KULLANILMAMIS

VESTEL	PROJECT NAME : 17mb185y-r1a	A3
SCH NAME :USB		T. SHT 8
DRAWN BY :<YOUR NAME HERE>		25/05/2022:10:34


HDMI1 (SIDE)
CN109
HDMI0_RX2P
HDMI0_RX2N
HDMI0_RX1P
HDMI0_RX1N
HDMI0_RX0P
HDMI0_RX0N
HDMI0_CLKP
HDMI0_CLKN
CEC
HDMI0_SCL
HDMI0_SDA
HDMI0_5V
5V_VCC
HOTPLUG0
Q130 BC848B
Q129 BC848B
R441 10Kohms
R440 10Kohms
R456 1Kohms
R457 1Kohms
R258 47Kohms
R259 47Kohms
R257 33ohms
R261 33ohms
R263 33ohms
TP2
TP3
TP4
TP5
TP6
HDMI2 (SIDE ARC)
CN110
HDMI2_RX2P
HDMI2_RX2N
HDMI2_RX1P
HDMI2_RX1N
HDMI2_RX0P
HDMI2_RX0N
HDMI2_CLKP
HDMI2_CLKN
HDMI_ARCP
HDMI2_SCL
HDMI2_SDA
HDMI2_5V
HOTPLUG2
HDMI_ARCN
Q132 BC848B
Q131 BC848B
R443 10Kohms
R442 10Kohms
R458 1Kohms
R459 1Kohms
R309
R314
R316 33ohms
R452 33ohms
R310 47Kohms
R311 47Kohms
R434 4.7Kohms
S153
TP8
TP12
TP13
TP14
e-ARC
R410 10Kohms
R415 47Kohms
200R
5.1K
0.022uH
L118
60R
F152
R411 10Kohms
R412 10Kohms
R416 47Kohms
1.2K
L119
F153
HDMI3 (SIDE)
CN1
R277 470ohms
DEBUG_RX
DEBUG_TX
HDMI1_RX2P
HDMI1_RX2N
HDMI1_RX1P
HDMI1_RX1N
HDMI1_RX0P
HDMI1_RX0N
HDMI1_CLKP
HDMI1_CLKN
HDMI1_SCL
HDMI1_SDA
HDMI1_5V
HOTPLUG1
C328 15pF 50V
R283 470ohms
R335 33ohms
R334
R333 33ohms
R336 47Kohms
R337 47Kohms
R47 1Kohms
R46 1Kohms
R445 10Kohms
R444 10Kohms
Q134 BC848B
Q133 BC848B
TP7
TP9
TP10
TP11
U108
MT9685LAAJAC
A_RX0N
A_RX0P
A_RX1N
A_RX1P
A_RX2N
A_RX2P
A_RXCN
A_RXCP
DDCDA_CK
DDCDA_DA
HOTPLUGA
HOTPLUGA_HDMI20_5V
B_RX0N
B_RX0P
B_RX1N
B_RX1P
B_RX2N
B_RX2P
B_RXCN
B_RXCP
DDCDB_CK
DDCDB_DA
HOTPLUGB
HOTPLUGB_HDMI20_5V
C_RX0N
C_RX0P
C_RX1N
C_RX1P
C_RX2N
C_RX2P
C_RXCN
C_RXCP
DDCDC_CK
DDCDC_DA
HOTPLUGC
HOTPLUGC_HDMI20_5V
D_RX0N
D_RX0P
D_RX1N
D_RX1P
D_RX2N
D_RX2P
D_RXCN
D_RXCP
DDCDD_CK
DDCDD_DA
HOTPLUGD
HOTPLUGD_HDMI20_5V
CEC0
NC
HDMIRX_ARCTXP
R262 33ohms
R453 33ohms
R315 33ohms
R454 33ohms
R332 33ohms
R455 33ohms
R308 100ohms
C442
C347
S151
LINEIN_L0
LINEIN_R0
LINEOUT_L0
LINEOUT_R0
EARPHONE_OUTL
EARPHONE_OUTR
VAG
VRM_ADC
I2S_OUT_MCK
I2S_OUT_BCK
I2S_OUT_WCK
I2S_OUT_SD0
I2S_OUT_SD1
I2S_OUT_SD2
SPDIF_IN
SPDIF_OUT
I2S_IN_BCK
I2S_IN_WCK
I2S_IN_DIN0
I2S_IN_DIN1
I2S_IN_DIN2
DMIC_BCK
DMIC_SD0
DMIC_SD1
DMIC_SD2
MICIN1
MICCM1
MICIN0
MICCM0
C323 0.0033uF
C322 0.0033uF
S144
S143
HP_LEFT
HP_RIGHT
CLOSE TO MSTAR IC
C296 0.1uF 16V
220R
F126
C319 12pF
C321 12pF
R255 22ohms
R254 22ohms
C318 12pF
AOLRCK
AOSDATA0
AOMCLK
AOBCK
AOLRCK_SW
AOSDATA0_SW
AOBCK_SW
4.7Kohms
R250
R12
AMP_PWR_CTL
3V3_VCC
S179
S180
MIC_MCK
MIC_D0
SYS_SCL
SYS_SDA
S13
S12
ALS_SCL
ALS_SDA
ETHERNET
CN112
ETH_TP
ETH_TN
ETH_RP
ETH_RN
TD+
TD-
RD+
RD-
TCT
RCT
NC1
NC2
SHLD1
SHLD2
C397
C25
1uF
CONN_RJ45_W/TRANSFORMER_SIDE_PIN
rj079-f08m2by-k
LED&IR&ALS
5V_VCC
F154 1k
3V3_VCC
F147 1k
C429 0.1uF
TP32
TP33
CN120
TP179
TP164
TP159
TP161
TP108
CN119
CN118
KEYBOARD_ONBOARD
GREEN_LED
RED_LED
3V3_STBY
D119
C5V6
F140 1k
IR_RC
C403 27pF 50V
R378 150ohms
LED2
R361 10Kohms
Q126 BC848B
R376 10Kohms
R377 220ohms
R370 220ohms
R379 10Kohms
Q128 BC858B
R447 10Kohms
R380 220ohms
Q127 BC848B
R362 10Kohms
LED1
DIMMING
TP110
BACKLIGHT_DIM
S106
DIMMING
KEYBOARD
KEYBOARD_ONBOARD
R342 10Kohms
3V3_STBY
R341 47ohms
1k
F133
PESD9N5VH
D132
1N5819
D11
0.1uF
C21
KEYBOARD
TP152
TACT SWITCH
TP101
R102 47ohms
KEYBOARD_ONBOARD
TP47
R101 4.7Kohms
C108 0.1uF 10V
D100
BZT52C5V6LP
SW100
SPDIF OUT
FB1
VIN
VCC
GND
SPDIF_COAX
S19
SW
F130 1k
5V_VCC
R318 4.7Kohms
C351 0.1uF 10V
Q120 BC848B
C357 0.1uF 10V
R324 100ohms
SPDIF_OUT
R317 4.7Kohms
C356 22pF 50V
TP148
SW
S8
JK1
TP145
C363 0.1uF 10V
C364 22pF 50V
R326 220ohms
R325 220ohms
VESTEL
PROJECT NAME : 17mb185y-r1a
A3
SCH NAME :HDMI_GPIO
T. SHT 8
DRAWN BY :<YOUR NAME HERE>
24/05/2022:10:05

1V8_VCC LDO

U120
LM1117
IN OUT
ADJ VOUT
3V3_VCC
1V8_VCC
C439 10uF 10V
C432 10uF 10V
C433 0.1uF 16V
TP186
D27

F149 220R
C425 0.1uF 16V
C426 0.1uF 16V

F118 60R
C181 10uF 10V
C180 0.1uF 16V
C176 0.1uF 16V
3V3_NAND

TP115
S32
5V_VCC
CI_PWR
C35 10uF 10V
C34 0.1uF 16V

C293 0.1uF
C294 0.1uF
C239 0.1uF
IF_P
IF_N
R219 10Kohms 0.1uF
F123 1k
3V3_TUNER
TUNER_IF_AGC
S129
C223 0.1uF
C366 0.1uF
C371 0.1uF
C358 0.1uF
C365 0.1uF
S152
S2_IP
S2_IN
S2_QP
S2_QN
S2_AGC

R299 4.7Kohms
R298 4.7Kohms
R300 4.7Kohms
R302 4.7Kohms
R11 4.7Kohms
3V3_VCC
SVS_SCL
SVS_SDA
PMIC_GPIO
R384 4.7Kohms
R383 4.7Kohms
3V3_VCC
DEMURA_WP

R394 10Kohms
R395 10Kohms
3V3_VCC
DOLBY VISION PORT

U108
MT9685LAAJAC

IP_T
IM_T
IFAGC_T
IP_S
IM_S
QP_S
QM_S
IFAGC_S
PCM2_IRQA_N_/_DISEQC_OUT
PCM2_RESET/_DISEQC_IN
DISEQC_OUT
TGPIO2_/_SCK1
TGPIO3_/_SDA1
TS2_CLK_/_SDIO_D0
TS2_SYNC_/_SDIO_D1
TS2_VLD_/_SDIO_D2
TS2_D0_/_SDIO_D3
PCM2_CE_N/SDIO_CLK
PCM2_CD_N/SDIO_CMD

EMMC_IO0_/_EMMC_D0_/_NAND-D4
EMMC_IO1_/_EMMC_D1_/_NAND-D3
EMMC_IO2_/_EMMC_D2_/_NAND-D2
EMMC_IO3_/_EMMC_D3_/_NAND-D5
EMMC_IO4_/_EMMC_D4_/_NAND-D6
EMMC_IO5_/_EMMC_D5_/_NAND-D7
EMMC_IO6_/_EMMC_D6_/_NAND-D0
EMMC_IO7_/_EMMC_D7_/_NAND-D1
EMMC_IO8_/_EMMC_DS_/_NAND-DQS
EMMC_IO9_/_EMMC_CMD_/_NAND_CEZ
EMMC_IO10_/_EMMC_CLK_/_NAND_REZ
EMMC_IO11_/_EMMC_RSTN_/_NAND_RBZ
EMMC_IO14_/_NAND_CLE
EMMC_IO15_/_NAND_ALE
EMMC_IO16_/_NAND_WEZ
EMMC_IO17_/_NAND_WPZ

PCM_A0 PCM_A1 PCM_A2 PCM_A3 PCM_A4 PCM_A5 PCM_A6 PCM_A7 PCM_A8 PCM_A9 PCM_A10 PCM_A11 PCM_A12 PCM_A13 PCM_A14
PCM_D0 PCM_D1 PCM_D2 PCM_D3 PCM_D4 PCM_D5 PCM_D6 PCM_D7
PCM_CD_N PCM_CE_N PCM_IORD_N PCM_IOWR_N PCM_IRQA_N PCM_OE_N PCM_REG_N PCM_RESET PCM_WAIT_N PCM_WE_N

TS0_D0 TS0_D1 TS0_D2 TS0_D3 TS0_D4 TS0_D5 TS0_D6 TS0_D7 TS0_CLK TS0_VLD TS0_SYNC
TS1_D0 TS1_D1 TS1_D2 TS1_D3 TS1_D4 TS1_D5 TS1_D6 TS1_D7 TS1_CLK TS1_VLD TS1_SYNC
PCM2_WAIT_N

R119 22ohms
R27 22ohms
R186 22ohms
R168 22ohms
R130 22ohms

U103
H26M41208HPR

EMMC_VIO
EMMC_CLK1
R390 4.7Kohms
R389 4.7Kohms
EMMC_CLK
EMMC_CMD
EMMC_D0 EMMC_D1 EMMC_D2 EMMC_D3 EMMC_D4 EMMC_D5 EMMC_D6 EMMC_D7
EMMC_RST
3V3_NAND
EMMC_VIO
C434 4.7uF
EMMC_DS
R391 4.7Kohms
R392 4.7Kohms
EMMC_D4 EMMC_D4 EMMC_D7
EMMC_D3
EMMC_D5 EMMC_D6
EMMC_D5 EMMC_D5

CI

CN104

R198 22ohms
R121 22ohms
R112 22ohms
R124 22ohms
R191 22ohms
R177 22ohms
R171 22ohms
R122 22ohms
R163 22ohms
R176 22ohms
R189 22ohms

PCM_A0 PCM_A1 PCM_A2 PCM_A3 PCM_A4 PCM_A5 PCM_A6 PCM_A7 PCM_A8 PCM_A9 PCM_A10 PCM_A11 PCM_A12 PCM_A13 PCM_A14
PCM_D0 PCM_D1 PCM_D2 PCM_D3 PCM_D4 PCM_D5 PCM_D6 PCM_D7
PCM_CD_N PCM_CE_N PCM_IORD_N PCM_IOWR_N PCM_IRQA_N PCM_OE_N PCM_REG_N PCM_RESET PCM_WAIT_N PCM_WE_N

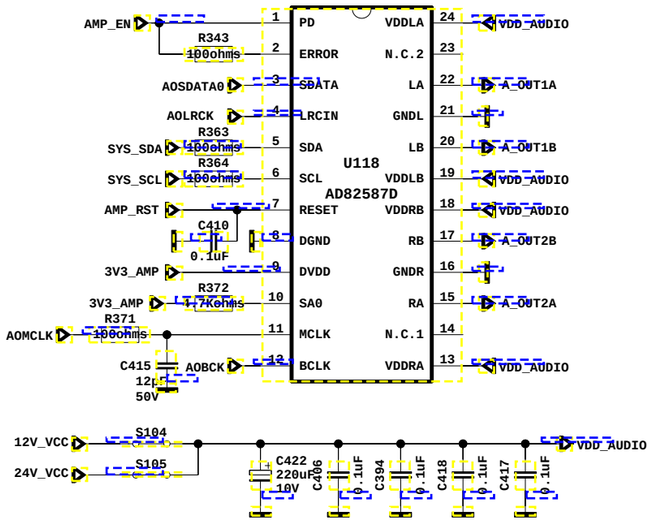
R110 10Kohms
1N4148 D104
1N4148 D101
PCM_CD1
PCM_CD2
PCM_CD

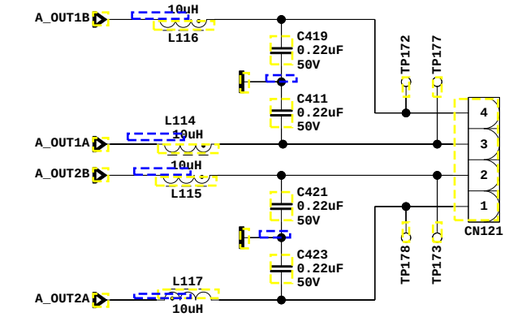
R188 22ohms
R180 10Kohms
R178 10Kohms
R179 10Kohms
R120 22ohms
R118 22ohms
R109 22ohms
R108 10Kohms
R134 22ohms
R123 10Kohms
R156 22ohms
R151 22ohms
R157 47Kohms
R117 10Kohms
C134 50V 10pF
C138 50V 10pF
C139 50V 10pF
C140 50V 10pF

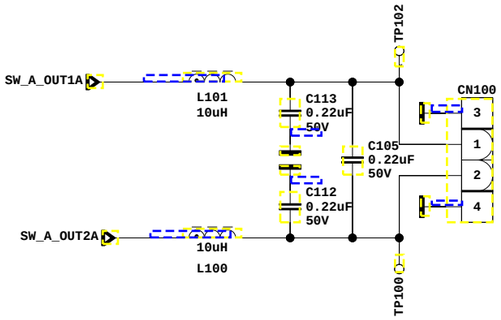
TS0_D0 TS0_D1 TS0_D2 TS0_D3 TS0_D4 TS0_D5 TS0_D6 TS0_D7 TS0_CLK TS0_VALID TS0_SYNC
TS1_D0 TS1_D1 TS1_D2 TS1_D3 TS1_D4 TS1_D5 TS1_D6 TS1_D7 TS1_CLK TS1_VALID TS1_SYNC
CI_A0 CI_A1 CI_A2 CI_A3 CI_A4 CI_A5 CI_A6 CI_A7 CI_A8 CI_A9 CI_A10 CI_A11 CI_A12 CI_A13 CI_A14
CI_D0 CI_D1 CI_D2 CI_D3 CI_D4 CI_D5 CI_D6 CI_D7
CI_IORD CI_IOWR CI_IRQA CI_OE CI_RST CI_WAIT CI_REG CI_WE CI_PWR

VESTEL	PROJECT NAME : 17mb185y-r1a		A3
SCH NAME :CI_EMMC		T. SHT	8
DRAWN BY :<YOUR NAME HERE>		24/05/2022:09:33	

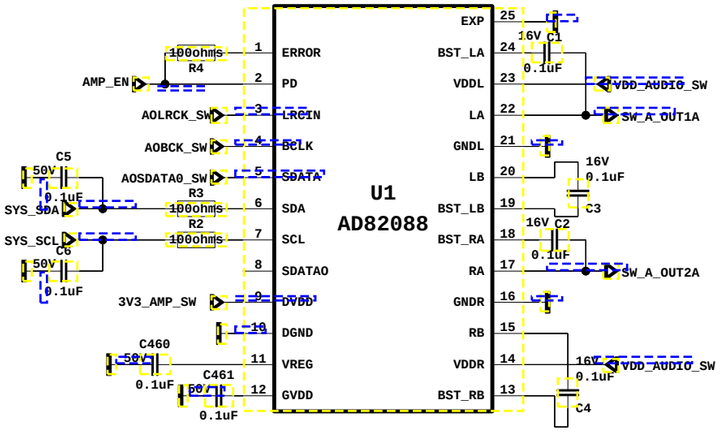
MAIN AMP
6W/8W/10W

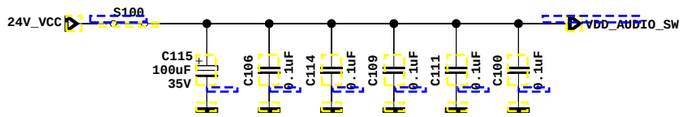


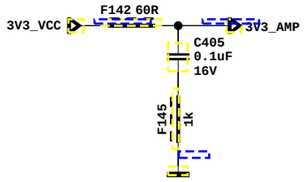


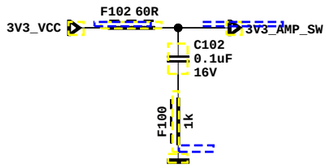


SUBWOOFER AMP

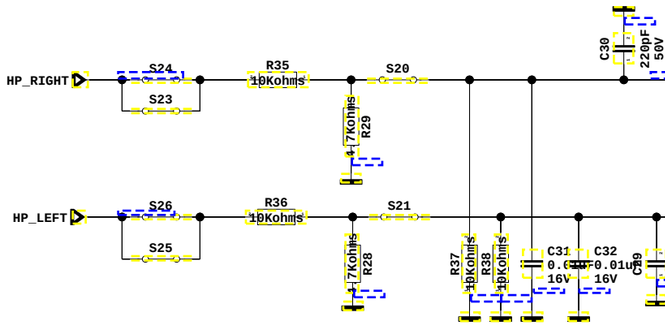




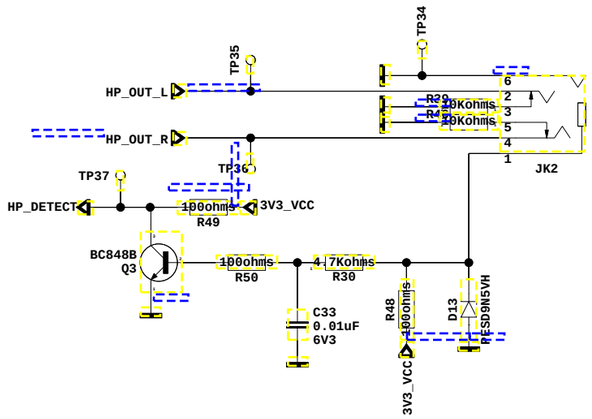




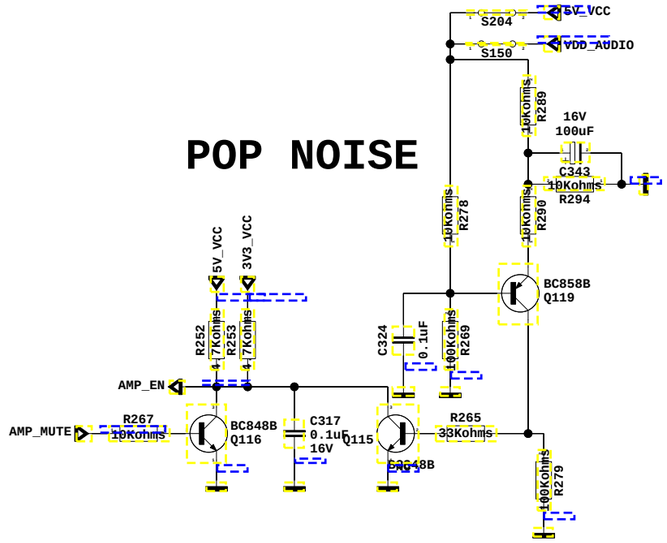
HEADPHONE



HEADPHONE OUTPUT



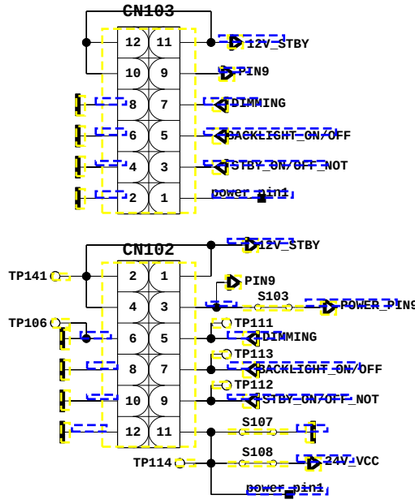
POP NOISE



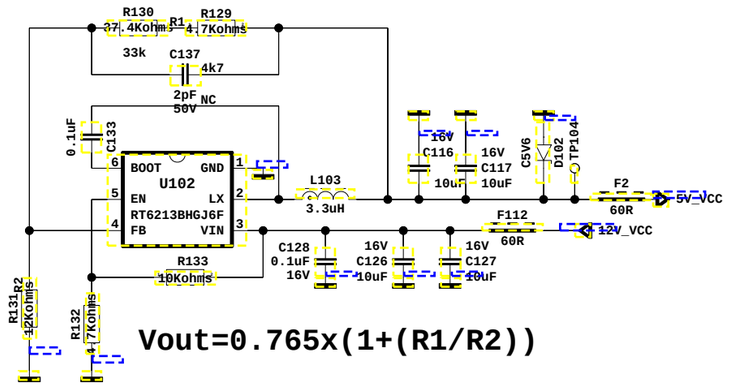
VESTEL	PROJECT NAME : 17mb185y-r1a	A3
	SCH NAME :AUDIO AMPs	T. SHT 8
	DRAWN BY :<YOUR NAME HERE>	24/05/2022:09:35

U108
MT9685LAAJAC
6
AVDD_DDR_A
AVDD_DDR_B
1V5_DRAM
16V 0.1uF C284
16V 0.1uF C291
AC28 J25 J26 L21 A16 H17 N15 N16 J14 K13
AVDD_DDR_DRAM_A-2 AVDD_DDR_DRAM_A-4 AVDD_DDR_DRAM_A-3 AVDD_DDR_DRAM_A-1 AVDD_DDR_DRAM_B-4 AVDD_DDR_DRAM_B-2 AVDD_DDR_VBP_A1 AVDD_DDR_VBN_A1 AVDD_DDR_VBP_B1 AVDD_DDR_VBN_B1
VDDC_CPU-10 VDDC_CPU-1 VDDC_CPU-2 VDDC_CPU-5 VDDC_CPU-6 VDDC_CPU-7 VDDC_CPU-8 VDDC_CPU-9 VDDC_CPU-4 VDDC_CPU-3
V13 V14 V15 V16 V17 W13 W14 W15 W16 W17
1V_VCC_CPU
1V_VCC_CPU 10 pins
VDDC 22 pins
VDDC_8 VDDC_20 VDDC_22 VDDC_4 VDDC_7 VDDC_6 VDDC_2 VDDC_18 VDDC_19 VDDC_17 VDDC_16 VDDC_11 VDDC_5 VDDC_3 VDDC_1 VDDC_10 VDDC_21 VDDC_9 VDDC_12 VDDC_13 VDDC_14 VDDC_15
R11 R12 T11 T12 P15 P16 P17 P18 R13 R14 R15 R16 R17 R18 R19 T13 T14 T15 T16 T17 T18 T19
1V_VCC_CORE
DVDD_DDR-1 DVDD_DDR-2 DVDD_DDR_RX_A DVDD_DDR_RX_B AVDDL_MOD-1 AVDDL_MOD-2
N13 P13 P14 N14 N12 P12
TP184 TP183
1V_VCC_CORE
AVDD_DDR_A-4 AVDD_DDR_A-1 AVDD_DDR_A-2 AVDD_DDR_A-3 AVDD_DDR_A-5
H27 K14 L14 M14 M13
1V5_DRAM
AVDD_DDR_B-5 AVDD_DDR_B-4 AVDD_DDR_B-1 AVDD_DDR_B-2 AVDD_DDR_B-3
A24 K12 L12 L11 M11
1V5_DRAM
AVDD_DDR_DRAM_A-6 AVDD_DDR_DRAM_A-5
B27 B28
1V5_DRAM
AVDD_DDR_DRAM_B-3 AVDD_DDR_DRAM_B-1
A27 B26
1V5_DRAM
AVDD_DDR_VBP_A AVDD_DDR_VBN_A
G28 J27
AVDD_DDR_VBP_A AVDD_DDR_VBN_A
AVDD_DDR_VBP_B AVDD_DDR_VBN_B
A25 B25
AVDD_DDR_VBP_B AVDD_DDR_VBN_B
AVDD_MOD_VTERM
A13
MOD_VTERM
AVDD_LDO_A
K11
AVDD_LDO
3V3_STANDBY-2 3V3_STANDBY-1 3V3_STANDBY-3
G1 G2 H3
3V3_STBY
VDDP-2 VDDP-1
AG8 AH8
3V3_VCC
AVDD_EMMC_3318-2 AVDD_EMMC_3318-1
AB24 AB25
1V8_VCC
NC-1 NC-2
A22 B21
DVDD_NODIE GND
F1 AG4
DVDD_NODIE
DVDD_3318-NAND, 2pins
20mA,20mil
1V8_VCC
C303 10uF 25V
C289 0.1uF 16V
C302 0.1uF 16V
R229 240ohms AC26 ZQ_A
R234 240ohms AC27 ZQ1_A
R232 240ohms G27 ZQ_B
R231 240ohms F28 ZQ1_B
1
DRAM_VREF_A M28 DRAM_VREF_A
DRAM_VREF_B D27 DRAM_VREF_B
U108
MT9685LAAJAC
NC C257 0.1uF
1V5_DRAM NC R228 1Kohms N28 A-RST
1V5_DRAM NC R226 1Kohms D26 B-RST
NC C279 0.1uF
TP136 L28 IO_CAL_AF]PLRF^
TP135 F27 IO_CAL_BF]PHRF^
GS102 GS100 GS104 GS101
1V_VCC_CPU
C208 10uF 25V
C238 0.1uF 16V
C256 0.1uF 16V
C237 0.1uF 16V
C255 0.1uF 16V
C222 0.1uF 16V
1V_VCC_CPU 10 pins
600mA,40mil
C236 0.1uF 16V
C254 0.1uF 16V
C235 0.1uF 16V
C253 0.1uF 16V
C221 0.1uF 16V
1V_VCC_CORE
VDDC 22 pins
3.8A,160mil
C184 10uF 25V
C206 0.1uF 16V
C211 0.1uF 16V
C213 0.1uF 16V
C217 0.1uF 16V
C218 0.1uF 16V
C232 0.1uF 16V
C196 0.1uF 16V
C212 0.1uF 16V
C252 0.1uF 16V
C233 0.1uF 16V
C219 0.1uF 16V
C201 0.1uF 16V
C205 0.1uF 16V
C200 0.1uF 16V
C249 0.1uF 16V
C231 0.1uF 16V
C264 0.1uF 16V
C250 0.1uF 16V
C234 0.1uF 16V
C251 0.1uF 16V
C193 0.1uF 16V
C220 0.1uF 16V
1V_VCC_CORE
DVDD_DDR
C210 0.1uF 16V
C199 0.1uF 16V
C194 0.1uF 16V
C198 0.1uF 16V
C193 10uF 25V
DVDD_DDR, 4 pins
3.8A,160mil
AVDDL_MOD, 2 pins
10mA,20mil
AVDDL_MOD
C203 0.1uF 16V
C204 0.1uF 16V
C187 10uF 25V
1V5_DRAM
C197 10uF 25V
C280 0.1uF 16V
C262 0.1uF 16V
C287 0.1uF 16V
C281 0.1uF 16V
C271 0.1uF 16V
C192 10uF 25V
C273 0.1uF 16V
C229 0.1uF 16V
C230 0.1uF 16V
C248 0.1uF 16V
C247 0.1uF 16V
C216 10uF 25V
C245 0.1uF 16V
C272 0.1uF 16V
C189 10uF 25V
C260 0.1uF 16V
C246 0.1uF 16V
250mA,25mil
AVDD_DDR_B, 5 pins
AVDD_DDR_A, 5 pins
AVDD_DRAM_B, 2 pins
AVDD_DRAM_A, 2 pins
1V8_VCC
0R S142
AVDD_LDO
C316 0.1uF 16V
AVDD_LDO, 1pin
20mA,20mil
DVDD_NODIE
C311 0.1uF 16V
C310 0.2uF 6V3
1V5_DRAM
C269 0.47uF 6V3
C263 0.47uF 6V3
AVDD_DDR_VBP_B
GND1
C270 0.47uF 6V3
AVDD_DDR_VBN_B
C282 0.47uF 6V3
AVDD_DDR_VBP_A
C274 0.47uF 6V3
AVDD_DDR_VBN_A
C281 0.47uF 6V3
MOD_VTERM option
1V_VCC_CORE
S141
MOD_VTERM
1V2_VCC
S140
0.1uF C300
1V2_VCC_VTERM
3V3_VCC
U109
TLV471P
IN OUT GND EN NC
1V2_VCC
C305 0.1uF 16V
3V3_STBY
AVDD_NODIE, 3pins
150mA,20mil
C309 0.1uF 16V
C313 0.1uF 16V
C314 0.1uF 16V
C315 0.1uF 16V
D124 PESD6N5VH
3V3_VCC
C304 0.1uF 16V
C301 0.1uF 16V
C290 0.1uF 16V
VDDP33, 2pins
150mA,20mil
1V5_DRAM
R227 1Kohms
R233 1Kohms
C288 0.1uF
C283 0.001uF
DRAM_VREF_A
1V5_DRAM
R225 1Kohms
R235 1Kohms
C278 0.1uF
C277 0.001uF
DRAM_VREF_B
GND-47 GND-48 GND-49 GND-50 GND-51 GND-52 GND-53 GND-54 GND-55 GND-56 GND-57 GND-58 GND-98 GND-99 GND-100 GND-101 GND-102 GND-59 GND-60 GND-61 GND-62 GND-63 GND-64 GND-65 GND-66 GND-67 GND-68 GND-69 GND-70 GND-71 GND-72 GND-89 GND-90 GND-91 GND-92 GND-73 GND-74 GND-75 GND-76 GND-77 GND-78 GND-79 GND-80 GND-81 GND-82 GND-83 GND-84 GND-85 GND-129 GND-128 GND-127 GND-130 GND-131 GND-132 GND-133 GND-134 GND-135 GND-136 GND-137 GND-138 GND-139 GND-140 GND-141 GND-142 GND-143 GND-144 GND-145 GND-146 GND-147 GND-148 GND-149 GND-150 GND-151 GND-152 GND-153 GND-154
L8 M8 M9 M10 M19 M20 M21 M23 M24 N4 N8 N9 N10 N11 N19 N20 N21 N22 N23 P8 P9 P11 P19 P20 P21 P22 R8 R9 R10 T3 T9 T10 U9 U10 U11 U12 U13 U14 U15 U16 U17 U18 U19 U23 U24 U25 V8 V9 V10 V11 V12 V18 W8 W9 W10 AA2 AB14 AC10 AD4 AD5 AD6 AD10 AD26 AE2 AE4 AE7 AE9 AE10 AE16 AE25 AF3 AF8 AF9 AF13 AH9 AH16 AH25
7
MT9685LAAJAC
U108
GND-1 GND-2 GND-3 GND-4 GND-5 GND-6 GND-7 GND-94 GND-95 GND-8 GND-9 GND-10 GND-11 GND-12 GND-13 GND-14 GND-15 GND-16 GND-17 GND-18 GND-93 GND-19 GND-20 GND-21 GND-22 GND-96 GND-97 GND-23 GND-24 GND-25 GND-26 GND-27 GND-28 GND-29 GND-30 GND-31 GND-32 GND-33 GND-34 GND-35 GND-36 GND-37 GND-38 GND-86 GND-87 GND-88 GND-39 GND-40 GND-41 GND-42 GND-43 GND-44 GND-45 GND-46 GND-103 GND-104 GND-105 GND-106 GND-107 GND-108 GND-109 GND-110 GND-111 GND-112 GND-113 GND-114 GND-115 GND-116 GND-117 GND-118 GND-119 GND-120 GND-121 GND-122 GND-123 GND-124 GND-125 GND-126
A2 A23 B13 B22 B23 B24 C7 C15 C21 C22 C24 C27 C28 D3 D13 D15 D19 D21 D22 D23 D24 E6 E13 E15 E19 E20 E21 E23 E24 E25 E26 F2 F10 F13 F15 F17 F18 F19 F20 F21 F23 F24 F26 G3 G6 G7 G8 G9 G10 G15 G17 G18 G19 G20 G21 G22 G24 G25 G26 H4 H13 H14 H15 H16 H18 H19 H20 H21 H25 H26 J7 J8 J9 J10 J12 K9 K10 K27
DRAM_VREF_A

VESTEL	PROJECT NAME : 17mb185y-r1a		A3
SCH NAME :MAIN_POWER		T. SHT	8
DRAWN BY :<YOUR NAME HERE>		24/05/2022:09:33	

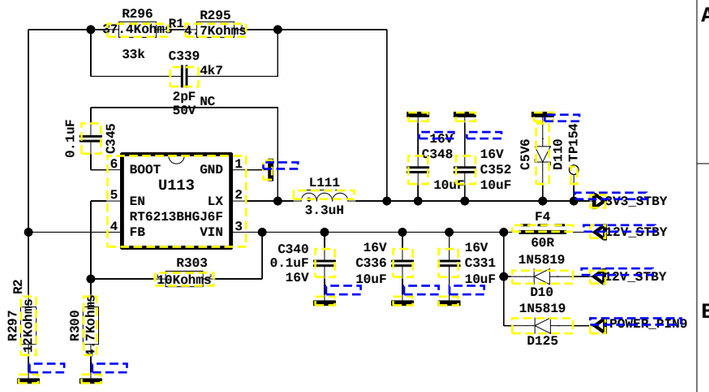


5V_VCC STEP-DOWN (3A)

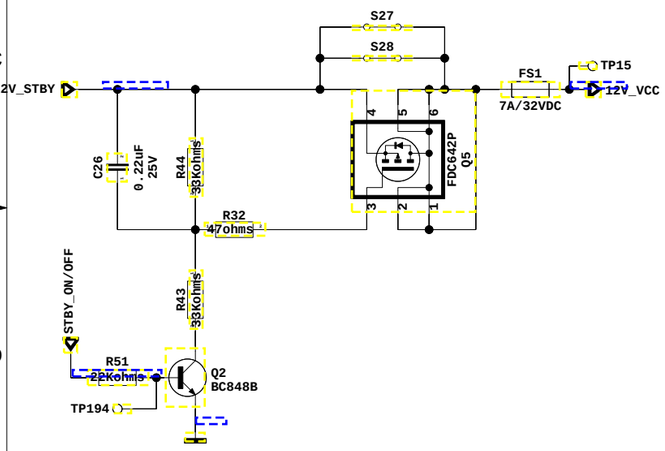


Vout=0.765x(1+(R1/R2))

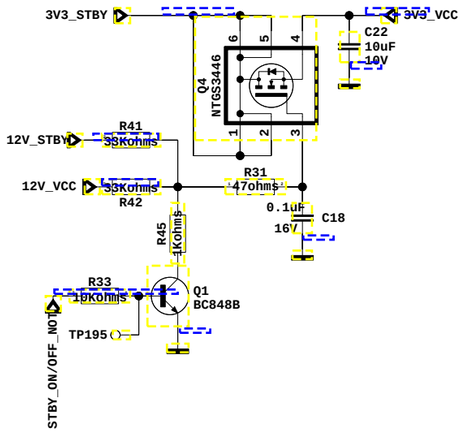
3V3_STBY DC/DC (2A)



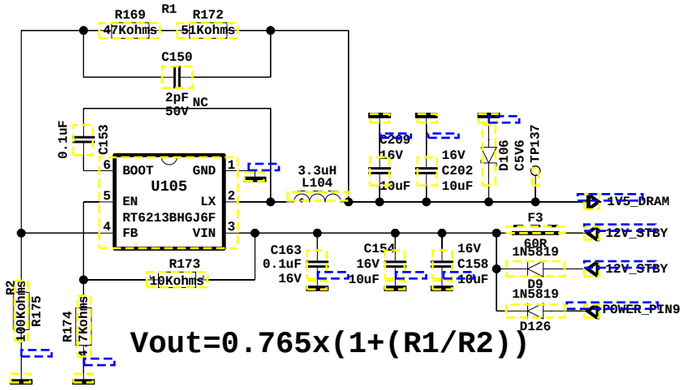
12V_VCC SWITCH



3V3_VCC SWITCH

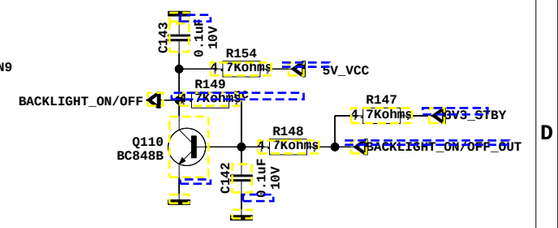


1V5_DRAM DC/DC (2A)

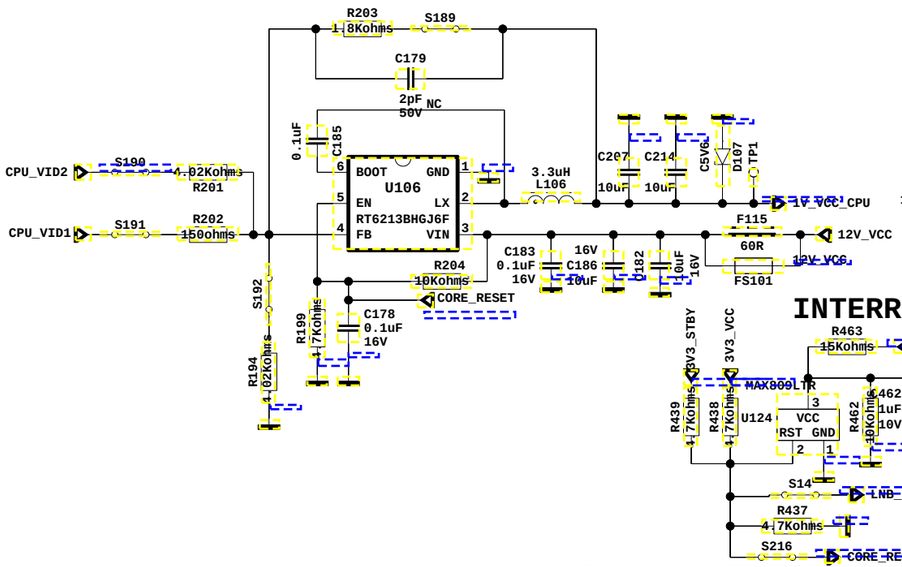


Vout=0.765x(1+(R1/R2))

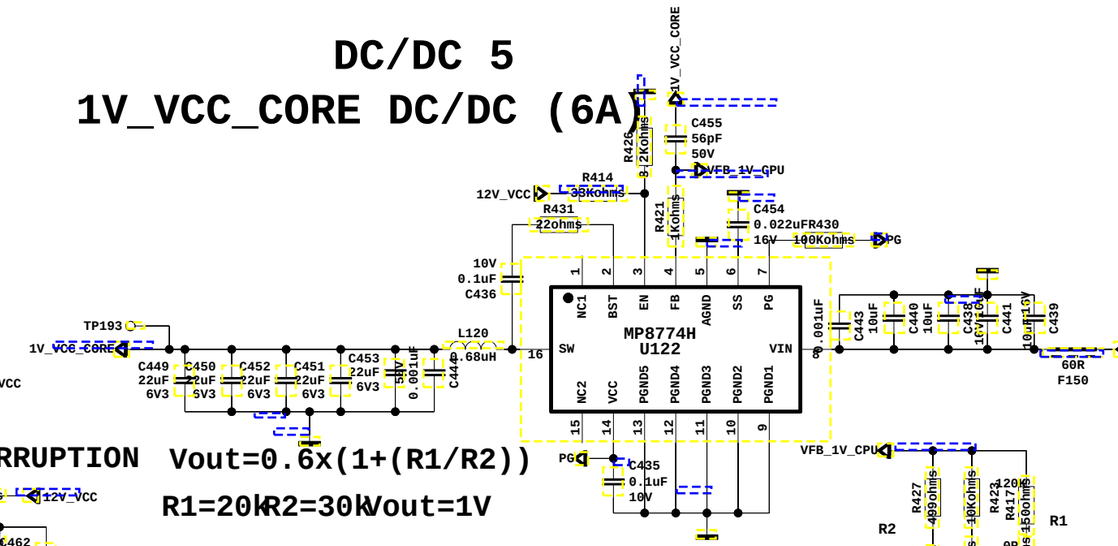
Backlight On/Off Circuit



1V_VCC_CPU DC/DC (2A)



DC/DC 5
1V_VCC_CORE DC/DC (6A)

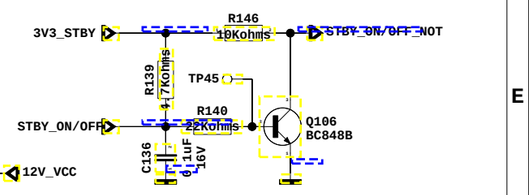


INTERRUPTION

Vout=0.6x(1+(R1/R2))

R1=20kR2=30kVout=1V

STBY On/Off Circuit



VESTEL	PROJECT NAME : 17mb185y-r1a	A3
SCH NAME :POWER		T. SHT 8
DRAWN BY :<YOUR NAME HERE>		24/05/2022:09:35