[CONTENTS]

SECTION 1. SUMMARY

❑ SERVICING PRECAUTIONS

❶ **Always disconnect the power source before:**

1) Removing or reinstalling any component, circuit board, module or any other instrument assembly.

2) Disconnecting or reconnecting any instrument electrical plug or other electrical connection.

3) Connecting a test substitute in parallel with an electrolytic capacitor in the instrument.

CAUTION: A wrong part substitution or incorrect polarity installation of electrolytic capacitors may result in an explosion hazard.

❷ **Do not defeat any plug/socket B+ voltage interlocks with which instruments covered by this service manual might be equipped.**

❸ **Do not apply power to this instrument and or any of its electrical assemblies unless all solid-state device heat sinks are correctly installed.**

❹ **Always connect a test instrument's ground lead to the instrument chassis ground before connecting the test instrument positive lead. Always remove the test instrument ground lead last.**

1) The service precautions are indicated or printed on the cabinet, chassis or components. When servicing, follow the printed or indicated service precautions and service materials.

2) The Components used in the unit have a specified conflammability and dielectric strength. When replacing any components, use components which have the same ratings. Components marked ⚠ in the circuit diagram are important for safety or for the characteristics of the unit. Always replace with the exact components.

3) An insulation tube or tape is sometimes used and some components are raised above the printed writing board for safety. The internal wiring is sometimes clamped to prevent contact with heating components. Install them as they were.

4) After servicing always check that the removed screws, components and wiring have been installed correctly and that the portion around the service part has not been damaged. Further check the insulation between the blades of attachment plug and accessible conductive parts.

❑ ESD PRECAUTIONS

[Electrostatically Sensitive Devices (ESD)]

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such omponents commonly are called Electrostatically Sensitive Devices (ESD). Examples of typical ESD devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

1) Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
2) After removing an electrical assembly equipped with ESD devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
3) Use only a grounded-tip soldering iron to solder or unsolder ESD devices.
4) Use only an anti-static solder removal device. Some solder removal devices not classified as “anti-static” can generate electrical charges sufficient to damage ESD devices.
5) Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ESD devices.
6) Do not remove a replacement ESD device from its protective package until immediately before you are ready to install it. (Most replacement ESD devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive material).
7) Immediately before removing the protective material from the leads of a replacement ESD device, touch the protective material to the chassis or circuit assembly into which the device will be installed.

   CAUTION: Be sure no power is applied to the chassis or circuit, and observe all other safety precautions.
8) Minimize bodily motions when handling unpackaged replacement ESD devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ESD device).

[CAUTION. GRAPHIC SYMBOLS]

	THE LIGHTNING FLASH WITH APROWHEAD SYMBOL. WITHIN AN EQUILATERAL TRIANGLE, IS INTENDED TO ALERT THE SERVICE PERSONNEL TO THE PRESENCE OF UNINSUBLATED “DANGEROUS VOLTAGE” THAT MAY BE OF SUFFICIENT MAGNITUDE TO CONSTITUTE A RISK OF ELECTRIC SHOCK.
	THE EXCLAMATION POINT WITHIN AN EQUILATERAL TRIANGLE IS INTENDED TO ALERT THE SERVICE PERSONNEL TO THE PRESENCE OF IMPORTANT SAFETY INFORMATION IN SERVICE LITERATURE.

❑ SPECIFICATIONS

1. GENERAL

Power requirements ..... DC12V~15V
Ground system ..... Negative
Dimensions(W x H x D) ..... 188 x 58 x 166mm
Weight ..... Net: 1.3kg

2. RADIO SECTION

	FM	AM(MW)
Frequency range	65.0~74.0MHz(Optional), 87.5~108MHz	522~1,620kHz (Optional:530~1,710kHz/ 520~1,620kHz)
Intermediate frequency	10.8MHz	450kHz
Usable sensitivity	12dBμV	32dBμV
Signal to noise ratio	55dB	45dB

3. COMPACT DISC SECTION

Frequency response ..... 40Hz~20kHz
Channel separation ..... 50dB(1kHz)
Signal to noise ratio 60dB

4. AUDIO SECTION

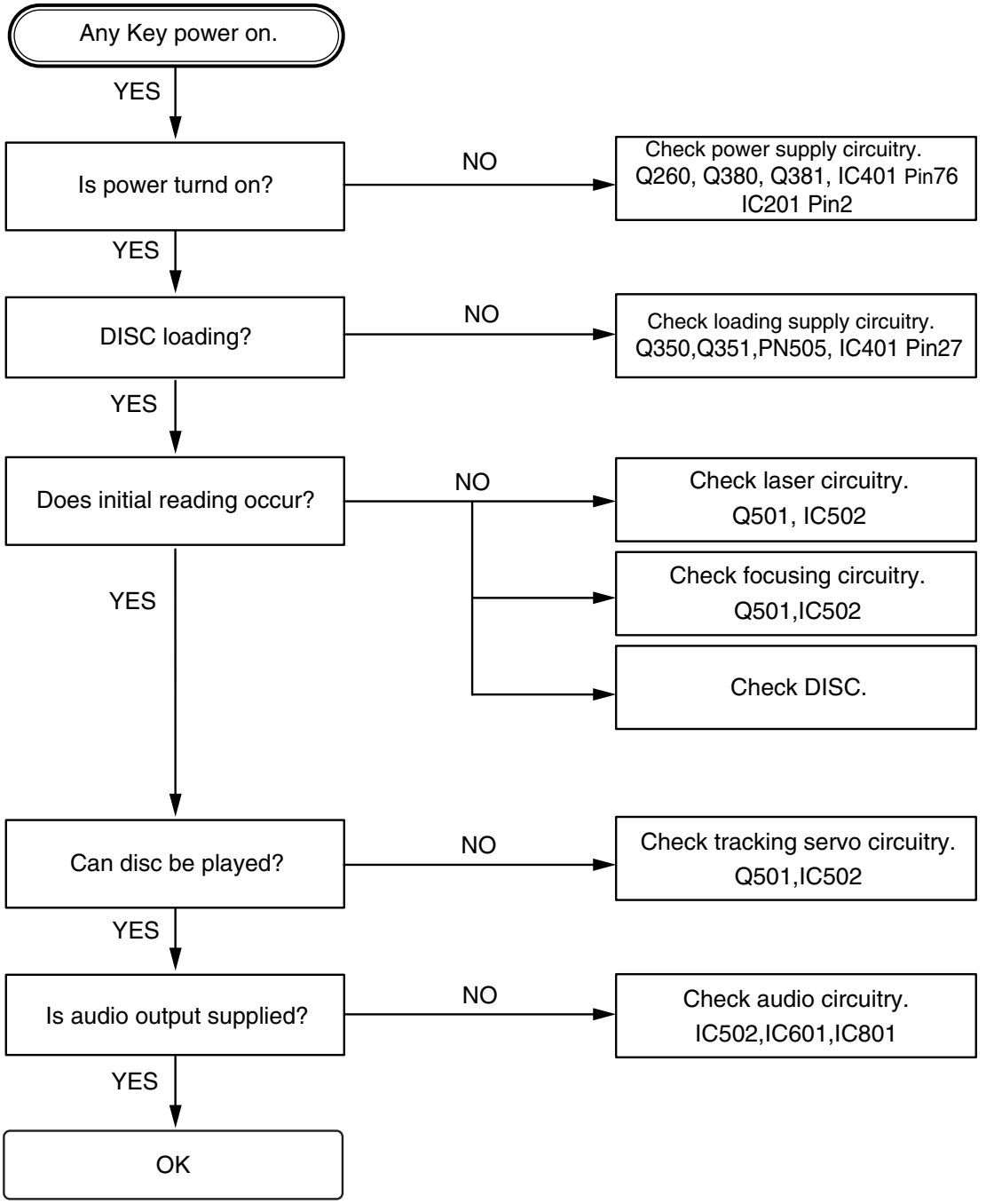
Maximum output power ..... 50W x 4
Speaker impedance ..... 4Ω x 4 or 8Ω x 4

NOTE: The design and specifications are subject to change without notice in the sourse of product improvement.

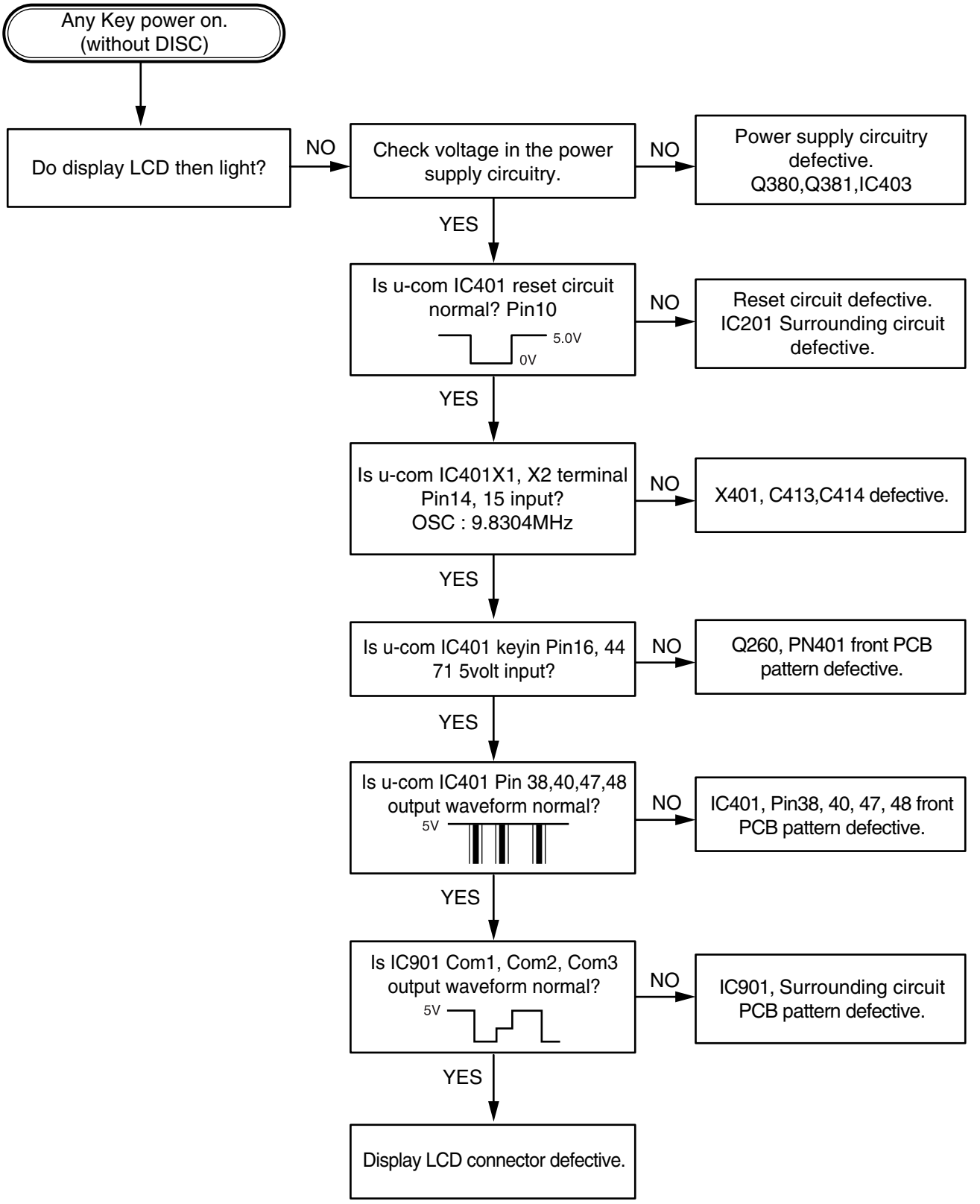
SECTION 2. ELECTRICAL

❑ ELECTRICAL TROUBLESHOOTING GUIDE

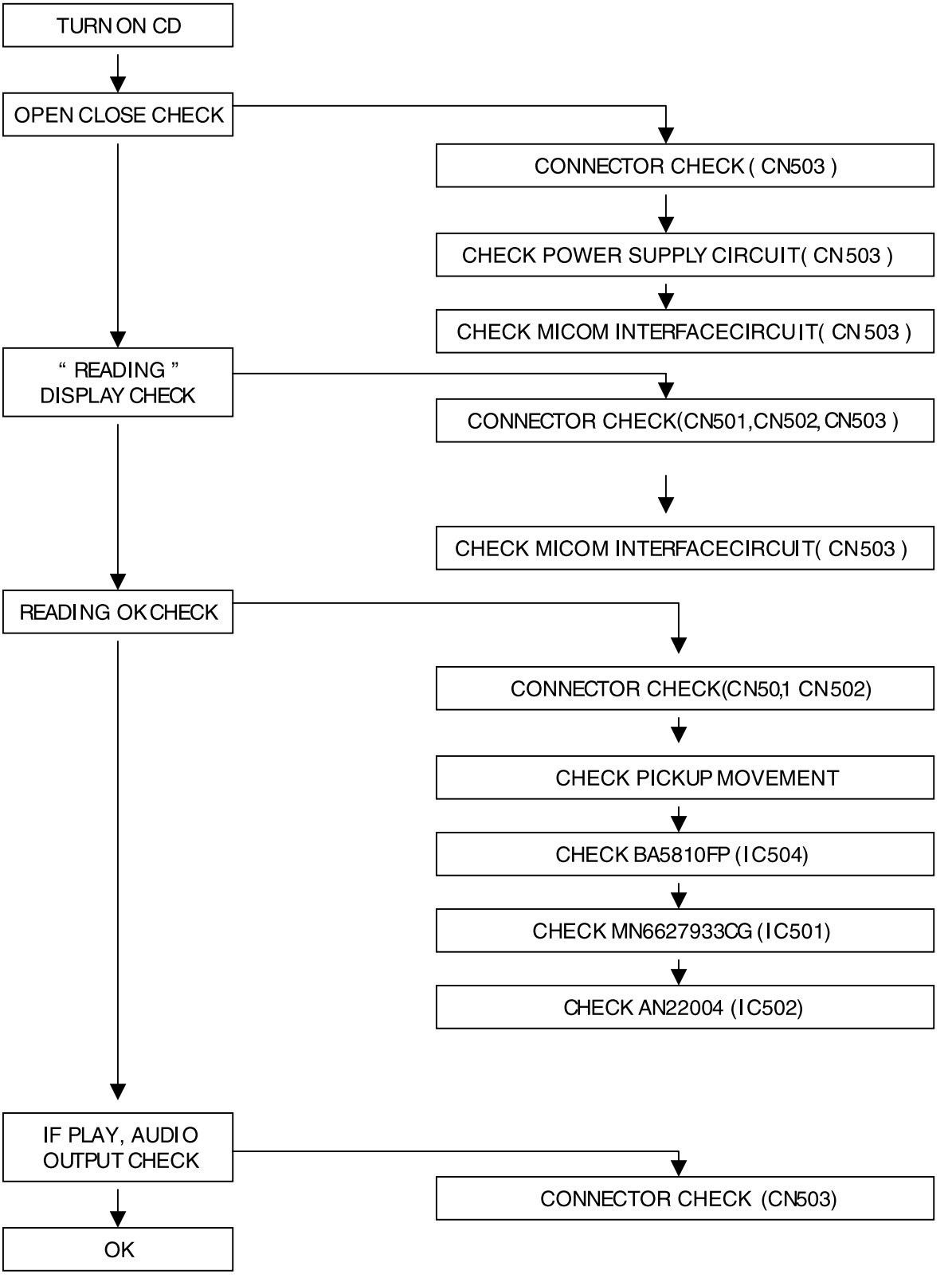
(1) No Power.



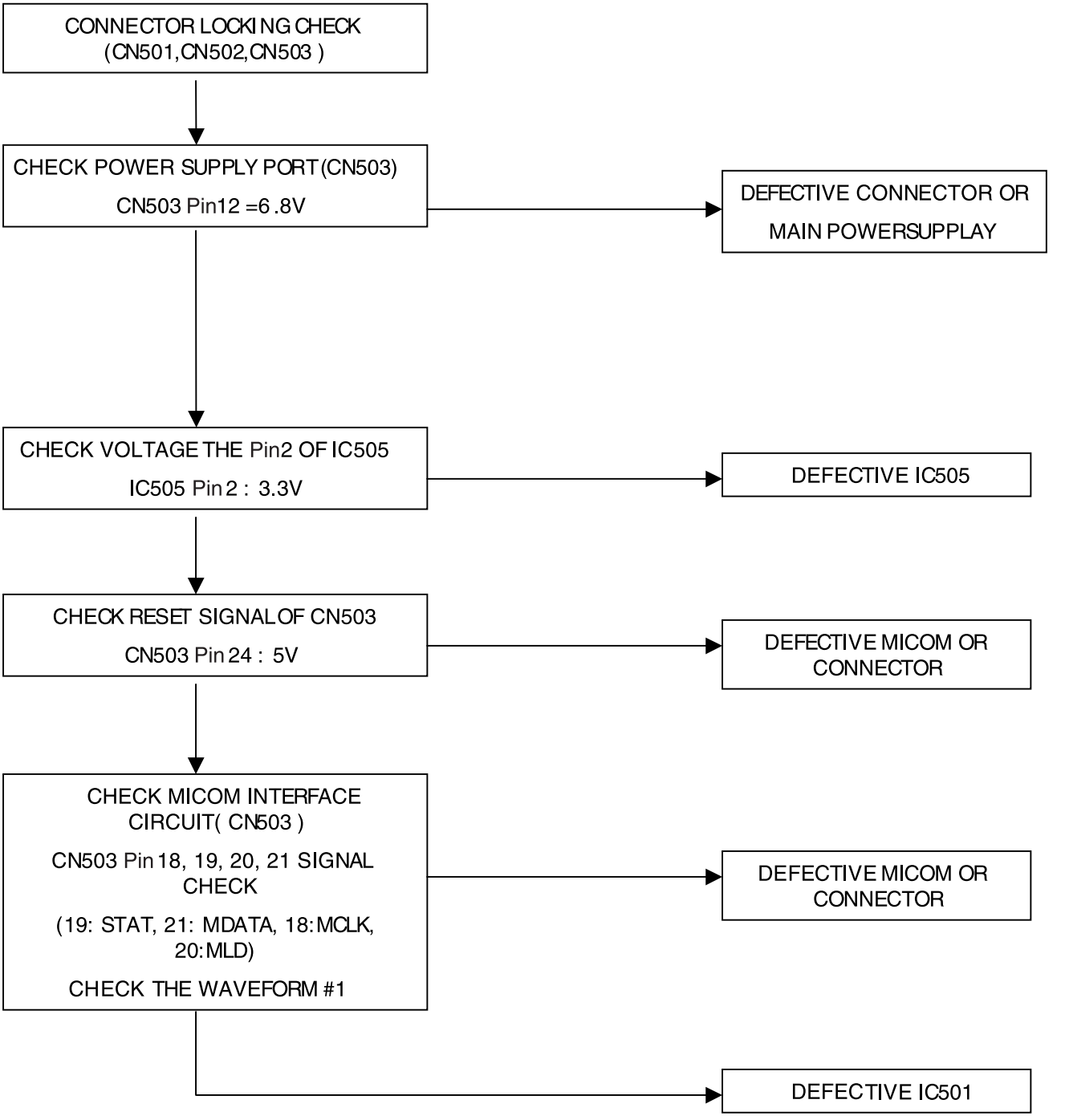
(2) LCD light abnornal.



CD PART

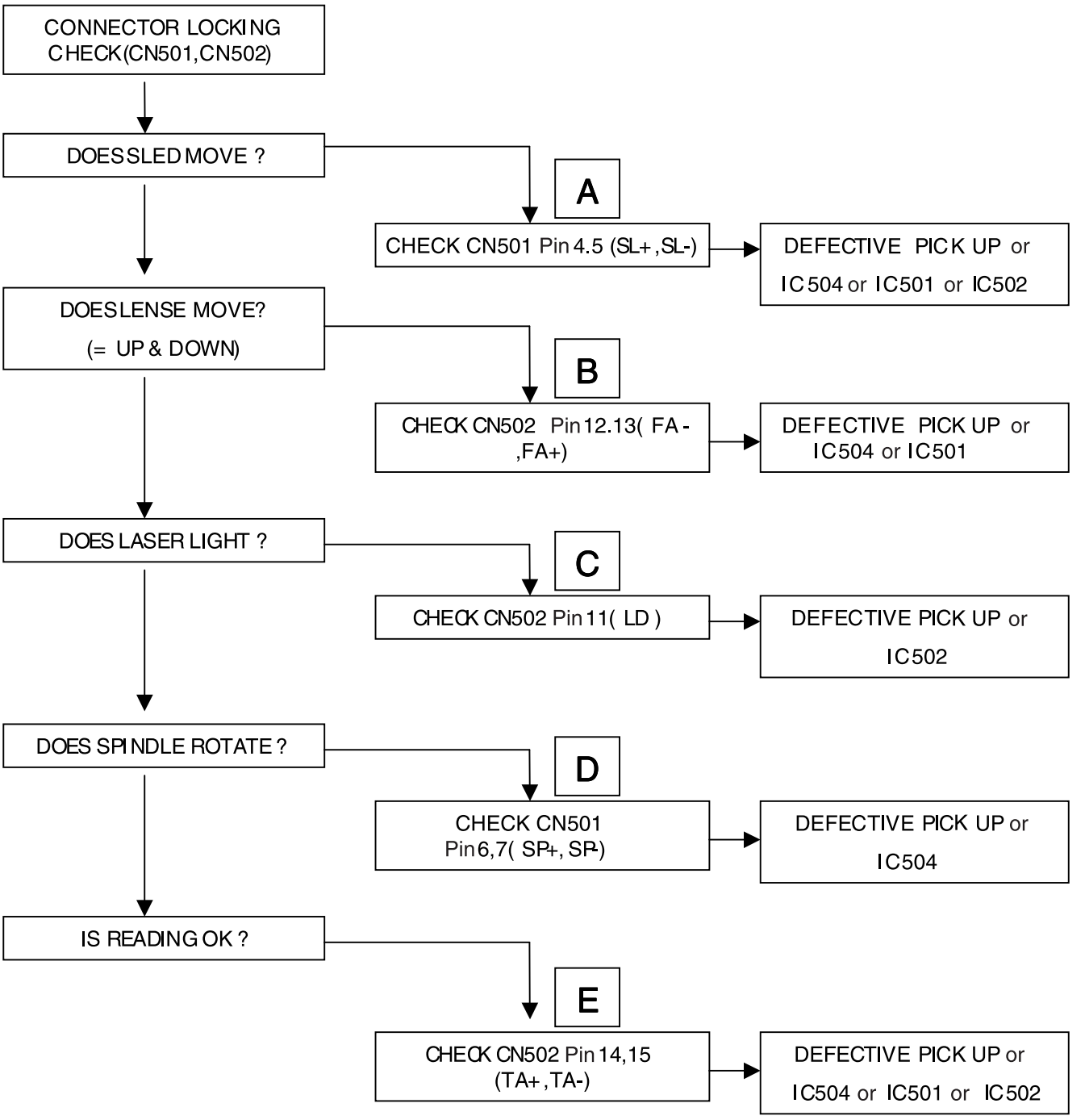

TURN ON CD
OPEN CLOSE CHECK
CONNECTOR CHECK (CN503)
CHECK POWER SUPPLY CIRCUIT(CN503)
CHECK MICOM INTERFACECIRCUIT(CN503)
“ READING ”
DISPLAY CHECK
CONNECTOR CHECK(CN501,CN502, CN503)
CHECK MICOM INTERFACECIRCUIT(CN503)
READING OK CHECK
CONNECTOR CHECK(CN501 CN502)
CHECK PICKUP MOVEMENT
CHECK BA5810FP (IC504)
CHECK MN6627933CG (IC501)
CHECK AN22004 (IC502)
IF PLAY, AUDIO
OUTPUT CHECK
CONNECTOR CHECK (CN503)
OK

" READING " DISPLAY CHECK
(= ONLY " CD " DISPLAY)



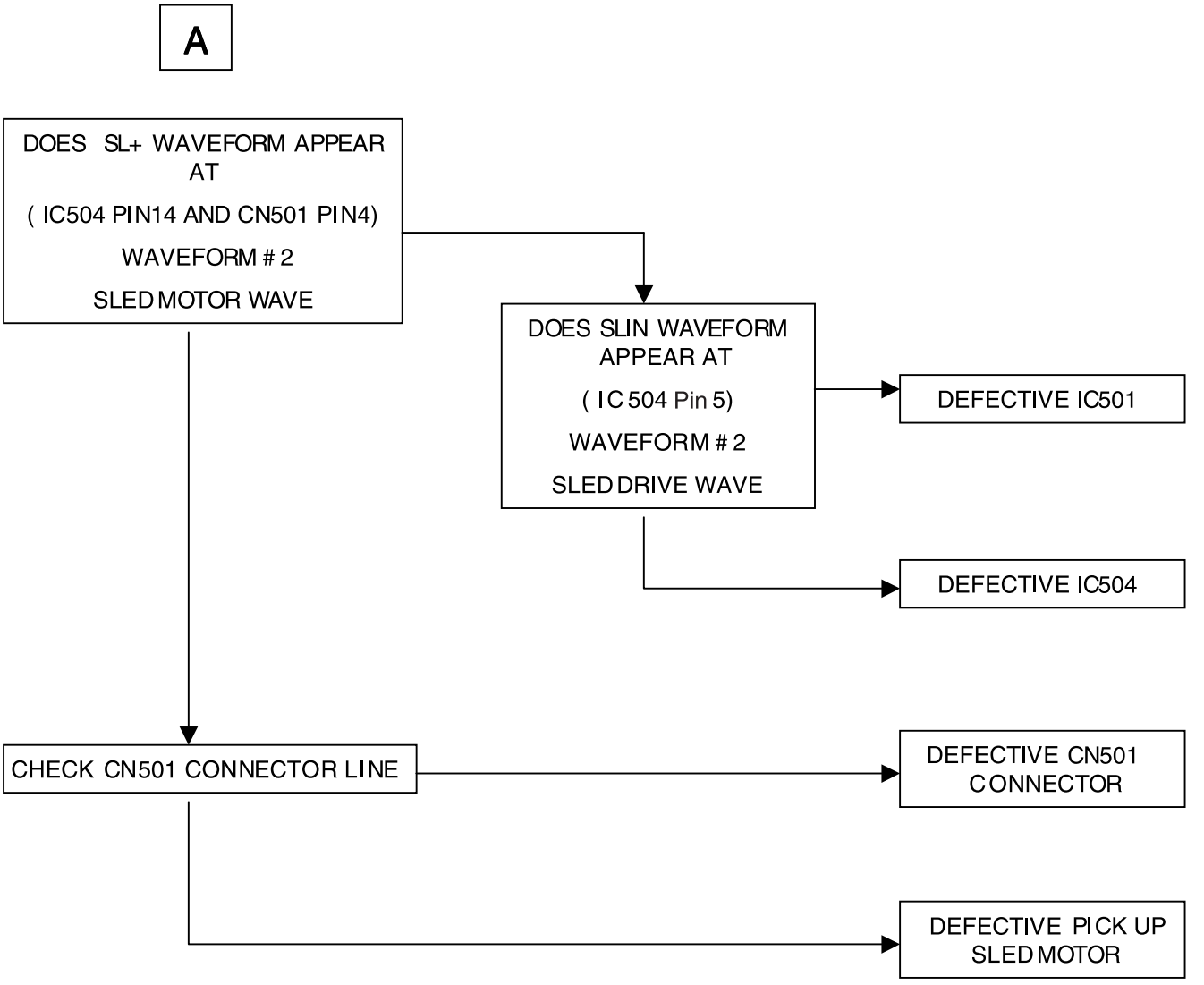
READING OK CHECK

(= “NO DISC” DISPLAY)



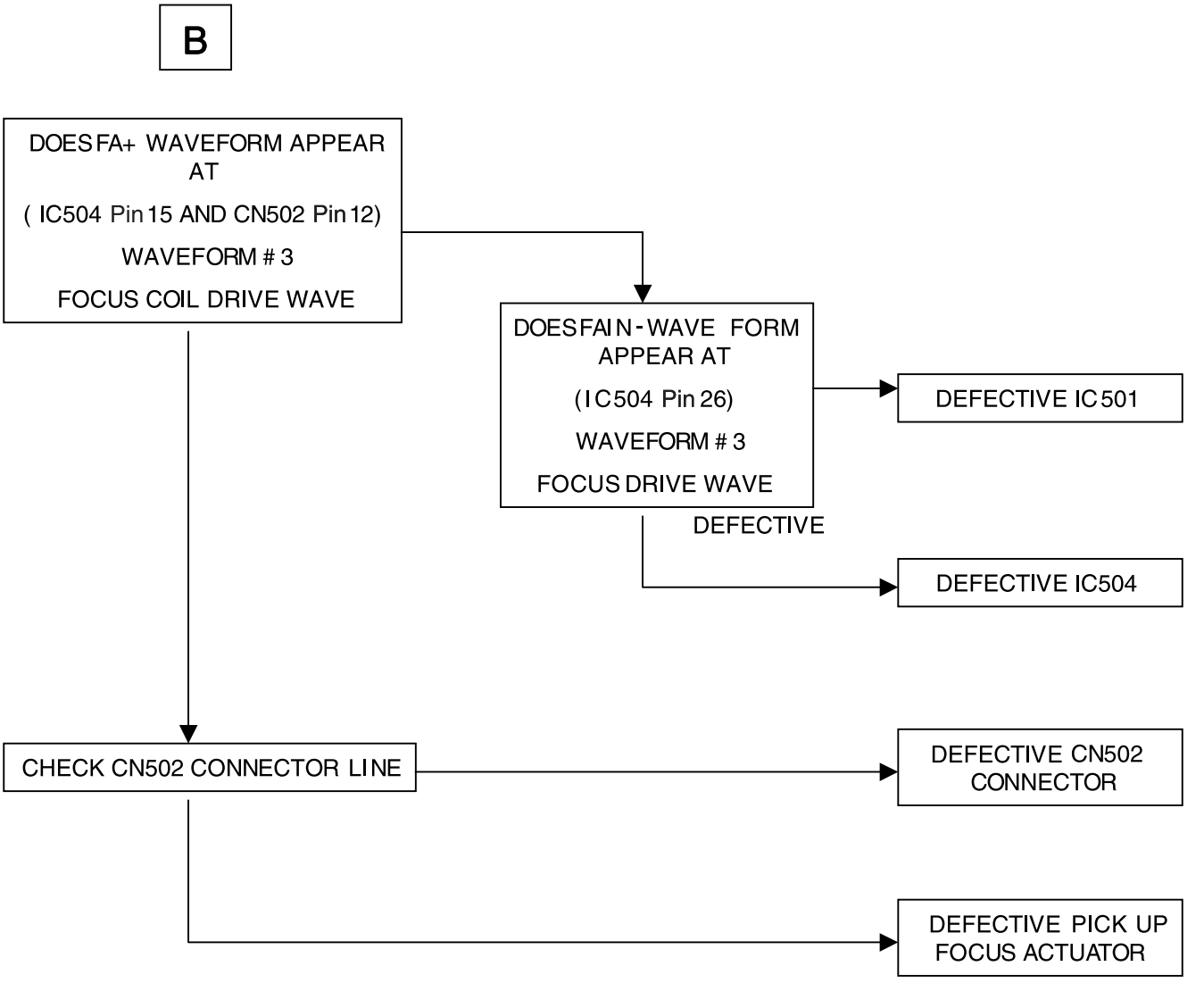
READING OK CHECK #A

(= “NO DISC” DISPLAY)



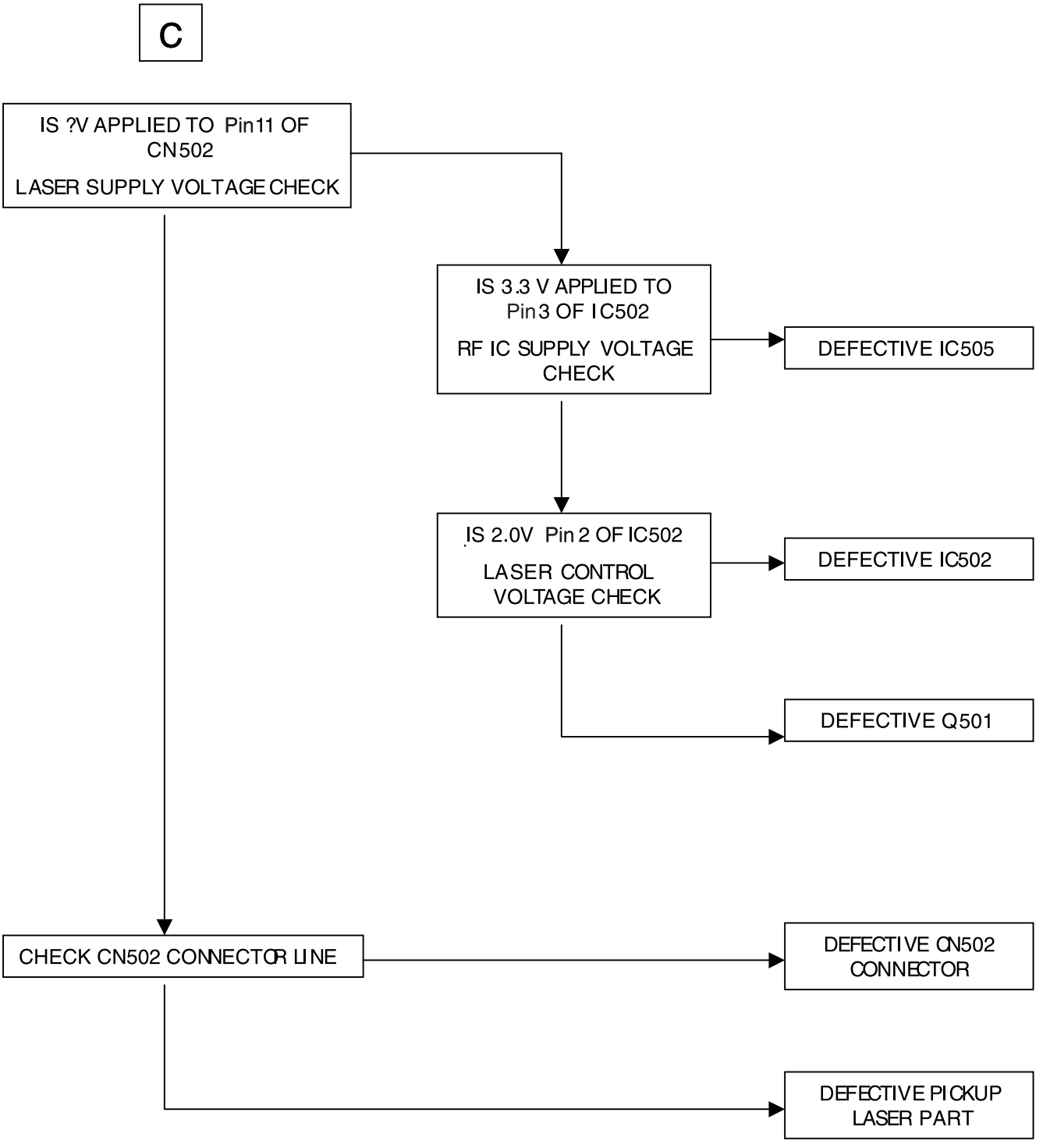
READING OK CHECK #B

(= “NO DISC” DISPLAY)



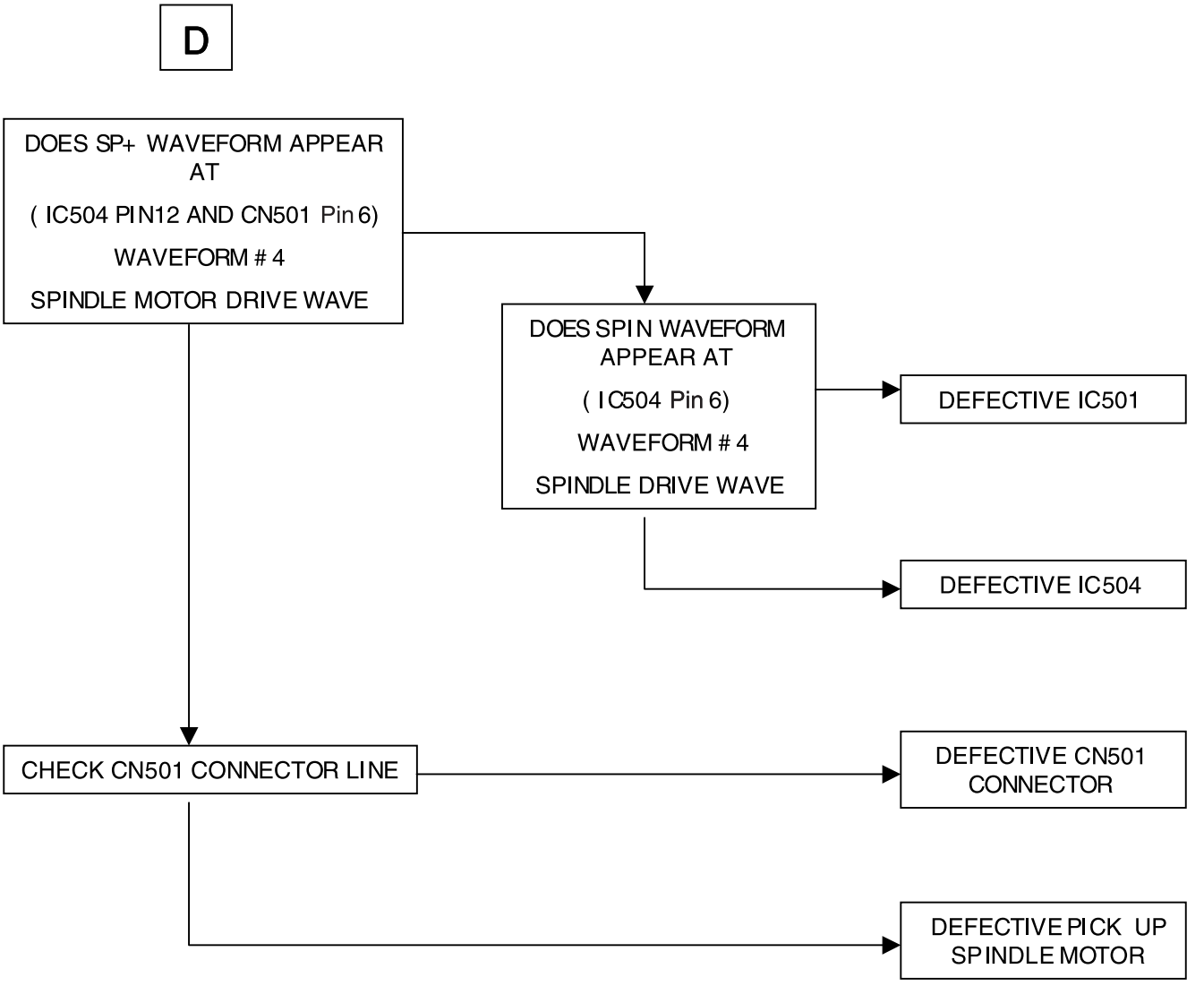
READING OK CHECK #C

(= “NO DISC” DISPLAY)



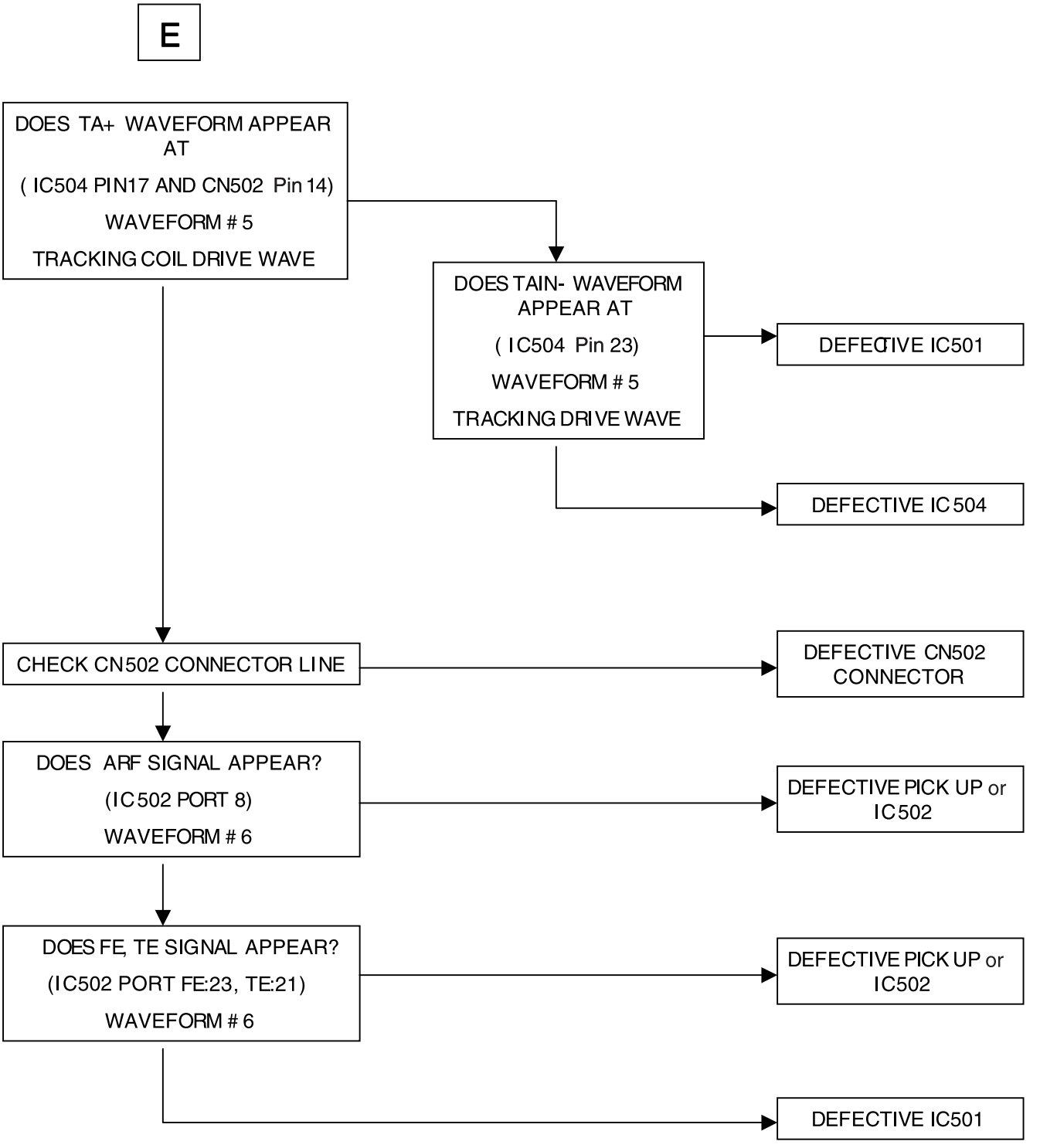
READING OK CHECK #D

(= “NO DISC” DISPLAY)



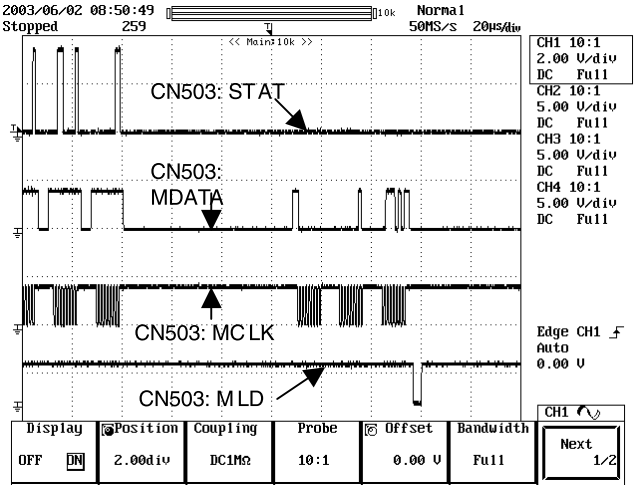
READING OK CHECK #E

(= “NO DISC” DISPLAY)

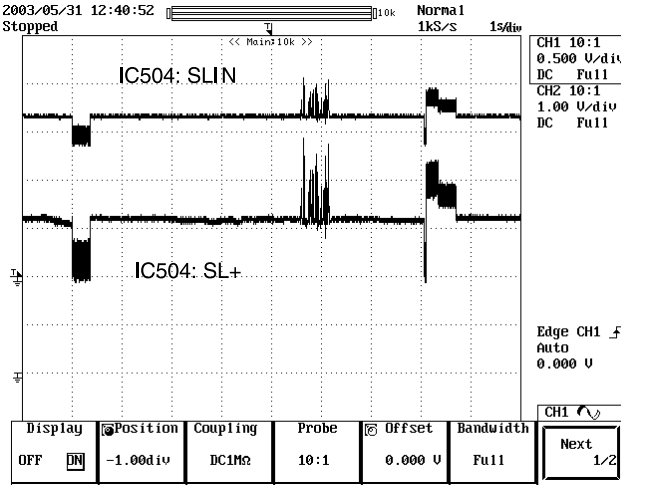


❑ WAVEFORMS OF MAJOR CHECK POINT

#1. MICOM INTERFACE WAVEFORM
(CN503 1 9,2 1 ,1 8,20) during normal play

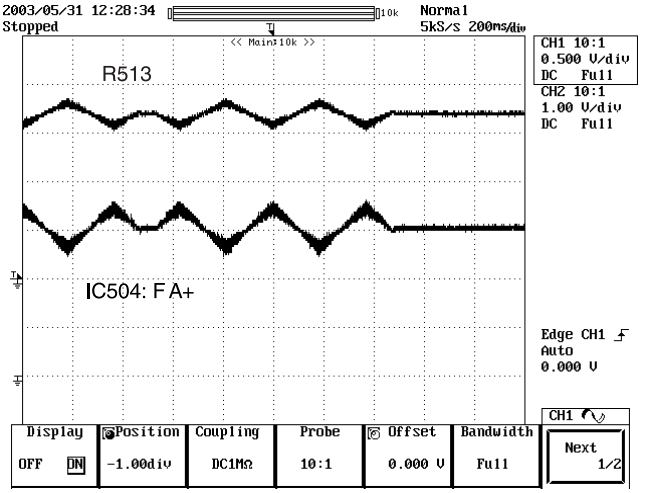


#2. SLED DRIVE AND MOTOR WAVEFORM
(IC504 pin5, 1 4) when focus search

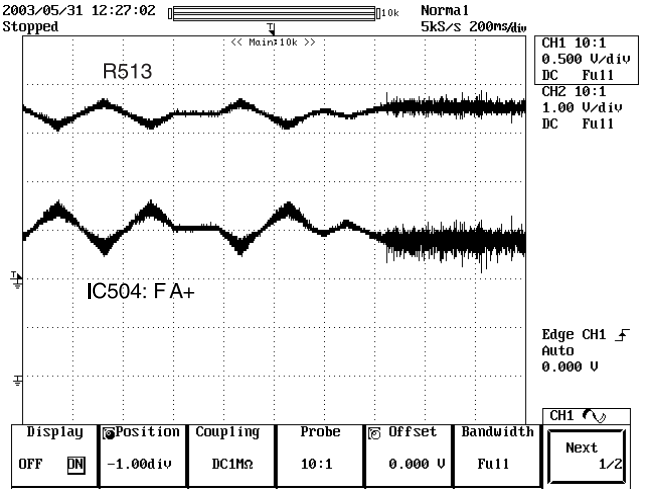


#3. FOCUS DRIVE AND MOTOR WAVEFORM
(R5 1 3, IC504 pin 1 5)

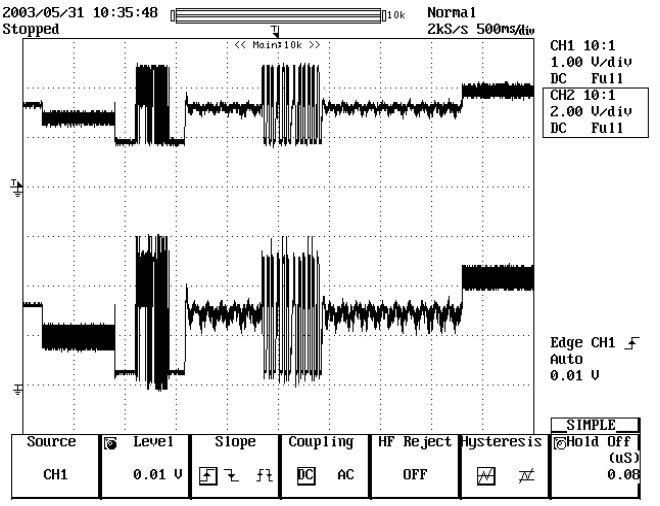
• When focus search failed or there is no disc on the tray



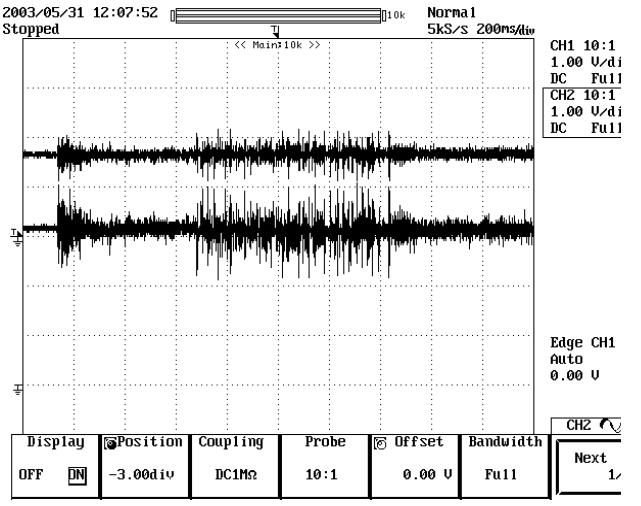
• There is disc on tray and focus search success



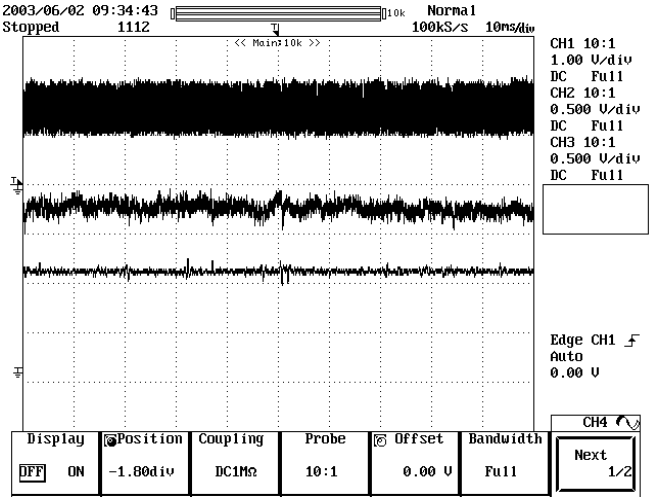
#4. SPINDLE DRIVE AND MOTOR WAVEFORM
(IC504 pin6, 1 2) when TOC reading



#5. TRACK DRIVE AND MOTOR WAVEFORM
(R508, IC504 pin23) during normal play



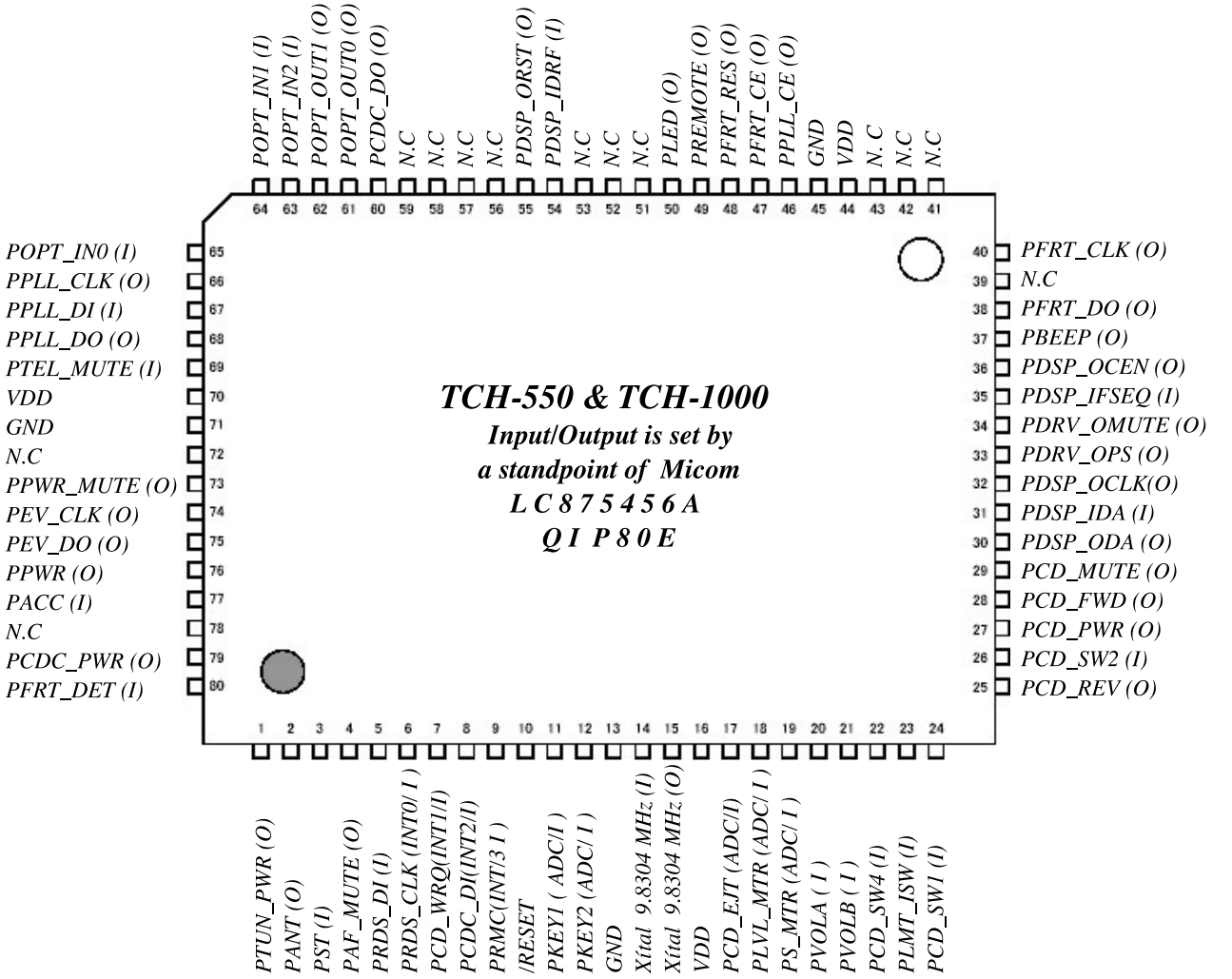
#6. RF, TRACKING AND FOCUS ERROR WAVEFORM
(IC502 pin8, 2 1 , 23) during normal play



❑ INTERNAL BLOCK DIAGRAM of ICs

■ IC401 LC875465B

1) PORT ASSIGNMENT



2) PORT DESCRIPTION

Pin	Name in Micom	Name in Model	I/O	Description
1	PA1/CS1#	PTUN_PWR	O	Tuner power supplier ON output Non RDS : Only in tuner function, it is set RDS : In all functions, it is set.
2	PA2/CS0#	PANT	O	Antenna control output When tuner is acting, Antenna is pulled out Antenna On(High), Antenna Off(Low)
3	PA3/WR#	PST	I	Stereo indigater's signal input Receive state : Stereo(Low), Mono(High) Search state : Station detect(High), Non station detect(Low)
4	PA4/RD#	PAF_MUTE	O	To tuner pack, AF mute ouput When reciever is switching to AF, Radio's audio output is muted Mute(High), Sound(Low)
5	PA5/RS	PRDS_DI	I	From tuner pack, RDS data input
6	P70/INT0/T0LCP/A	PRDS_CLK	I	From tuner pack, RDS clock input(interrupt0) 1187.5Hz ± 0.125 bit-rate clock
7	P71/INT1/T0HCP/	PCD_IWRQ	I	Sub-Q read standard level signal input(interrupt1), Low Active.
8	P72/INT2/T0IN	PCDC_DI	I	From CD changer, data input(interrupt2)
9	P73/INT3/T0IN	PRMC *	I	Remote Controller's signal input(interrupt3)
10	RES#	RESET	I	Reset
11	XT1/AN10	PKEY1	I	Key #1 line input(AD converter10 used)
12	XT2/AN11	PKEY2	I	Key #2 line input(AD converter11 used)
13	VSS1	GND	-	Ground
14	CF1	CF1	I	Xital 9.8304 MHz
15	CF2	CF2	O	Xital 9.8304 MHz
16	VDD1	VDD	-	Power supply (+5V)
17	P80/AN0	PCD_EJT *	I	CD Eject key input(AD converter 0 used) Seperated port is used (Under 3.76V)
18	P81/AN1	PLVL_MTR	I	Sound level's signal input(AD converter 1 used)
19	P82/AN2	PS_MTR	I	Radio station's strength signal input(AD converter 2 used)
20	P83/AN3	PVOLA	I	Encoder volume terminal #A input
21	P84/AN4	PVOLB	I	Encoder volume terminal #B input Clockwise PVOLA ① ② ③ ④ — ① ② ③ ④ = H H L L PVOLB — H L L H Counter-clockwise PVOLA ① ② ③ ④ — ① ② ③ ④ = H L L H PVOLB — H H L L When PVOLA & PVOLB's state is turned from ① to ① again like below, Volume level is changed to ① → ② → ③ → ④
22	P85/AN5	PCD_SW4	I	In MD, SW4 state input. Refer to CD Player.
23	P86/AN6	PCD_LMT_ISW	I	In MD, limit switch state input Being Pick-Up innermost position(High), The Others(Low)
24	P87/AN7	PCD_SW1	I	In MD, SW1 state input. Refer to CD Player.
25	P30	PCD_REV	O	In MD, load motor "reverse" command output

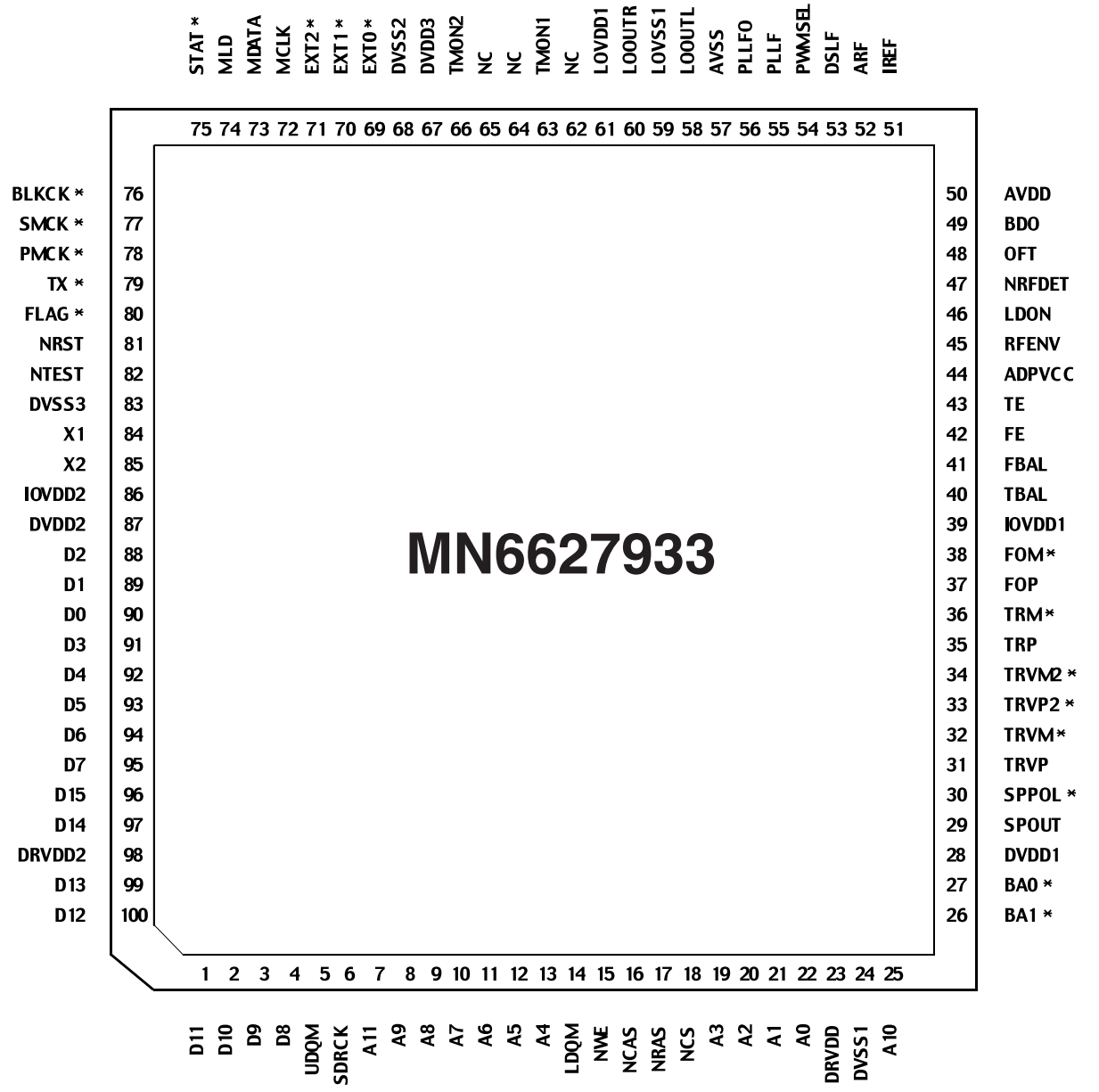
PCD_F	PCD_R	Function
Low	Low	Open mode
Low	High	Reverse
High	Low	Forward
High	High	Break mode

Pin	Name in Micom	Name in Model	I/O	Description
26	P31	PCD_SW2	I	In MD, SW2 state input. Refer to CD Player.
27	P32	PCD_PWR	O	DSP power suppler ON ouptut
28	P33	PCD_FWD	O	In MD, load motor "forward" command output PCD_F / PCD_R / Function Low / Low / Open mode Low / High / Reverse High / Low / Forward High / High / Break mode
29	P34	PCD_MUTE	O	CD's audio signal mute output
30	P10/SO0	PDSP_ODA	O	To DSP, data output
31	P11/SI0/SB0	PDSP_IDA	I	From DSP, data input
32	P12/SCK0	PDSP_OCLK	O	Clock output for interface with DSP
33	P13/SO1	PDRV_OPS	O	In MD, motor driver's power save command ouput Power Save Mode(High), Normal Mode(Low)
34	P14/SI1/SB1	PDRV_OMUTE	O	In MD, all motor's output "cut off" command ouput Cut Off Mode(High), Normal Mode(Low)
35	P15/SCK1	PDSP_IFSEQ	I	Constant velocity signal input Ok(High), Not Ok(Low)
36	P16/T1PWML	PDSP_OCEN	O	DSP chip enable output
37	P17/T1PWMH/BU	PBEEP	O	Beep sound (2KHz) output
38	SI2P0/SO2	PFRT_DO	O	To LCD driver, data output
39	SI2P1/SI2/SB2	N.C	I	Not to be used
40	SI2P2/SCK2	PFRT_CLK	O	Clock output for interface with LCD driver
41	SI2P3/SCK20	N.C	I	Not to be used
42	PWM1	N.C	O	Not to be used
43	PWM0	N.C	O	Not to be used
44	VDD2	VDD	-	Power supply (+5V)
45	VSS2	GND	-	Ground
46	P00	PPLL_CE	O	PLL IC enable output
47	P01	PFRT_CE	O	LCD driver enable output
48	P02	PFRT_RES	O	LCD driver reset output Normal(High), Reset(Low)
49	P03	PREMOTE	O	External amplifier ON output
50	P04	PLED	O	LED flashing control output
51	P05	N.C	O	Not to be used
52	P06	N.C	O	Not to be used
53	P07	N.C	O	Not to be used
54	P20/INT4/T1IN	PDSP_IDRF	I	Focusing OK signal input Ok(High), Not Ok(Low)
55	P21/INT4/T1IN	PDSP_IRST	O	DSP reset output
56	P22/INT4/T1IN	N.C	I	Not to be used
57	P23/INT4/T1IN	N.C	I	Not to be used
58	P24/INT5/T1IN	N.C	I	Not to be used
59	P25/INT5/T1IN	N.C	I	Not to be used
60	P26/INT5/T1IN	PCDC_DO	O	To CD changer, data output
61	P27/INT5/T1IN	POPT_OUT0	O	For diode option check, signal 1 output. Refer to Option Diode.
62	PB7/D7	POPT_OUT1	O	For diode option check, signal 2 output. Refer to Option Diode.
63	PB6/D6	POPT_IN2	I	For diode option check, signal 1 or 2 input2. Refer to Option Diode.
64	PB5/D5	POPT_IN1	I	For diode option check, signal 1 or 2 input1. Refer to Option Diode.
65	PB4/D4	POPT_IN0	I	For diode option check, signal 1 or 2 input0. Refer to Option Diode.
66	PB3/D3	PPLL_CLK	O	Clock output for interface with PLL IC
67	PB2/D2	PPLL_DI	I	From PLL IC, data input
68	PB1/D1	PPLL_DO	O	To PLL IC, data output
69	PB0/D0	PTEL_MUTE	I	Telephone mute input
70	VSS3	GND	-	Ground
71	VDD3	VDD	-	Power supply (+5V)
72	PC7/A7	N.C	I	Not to be used

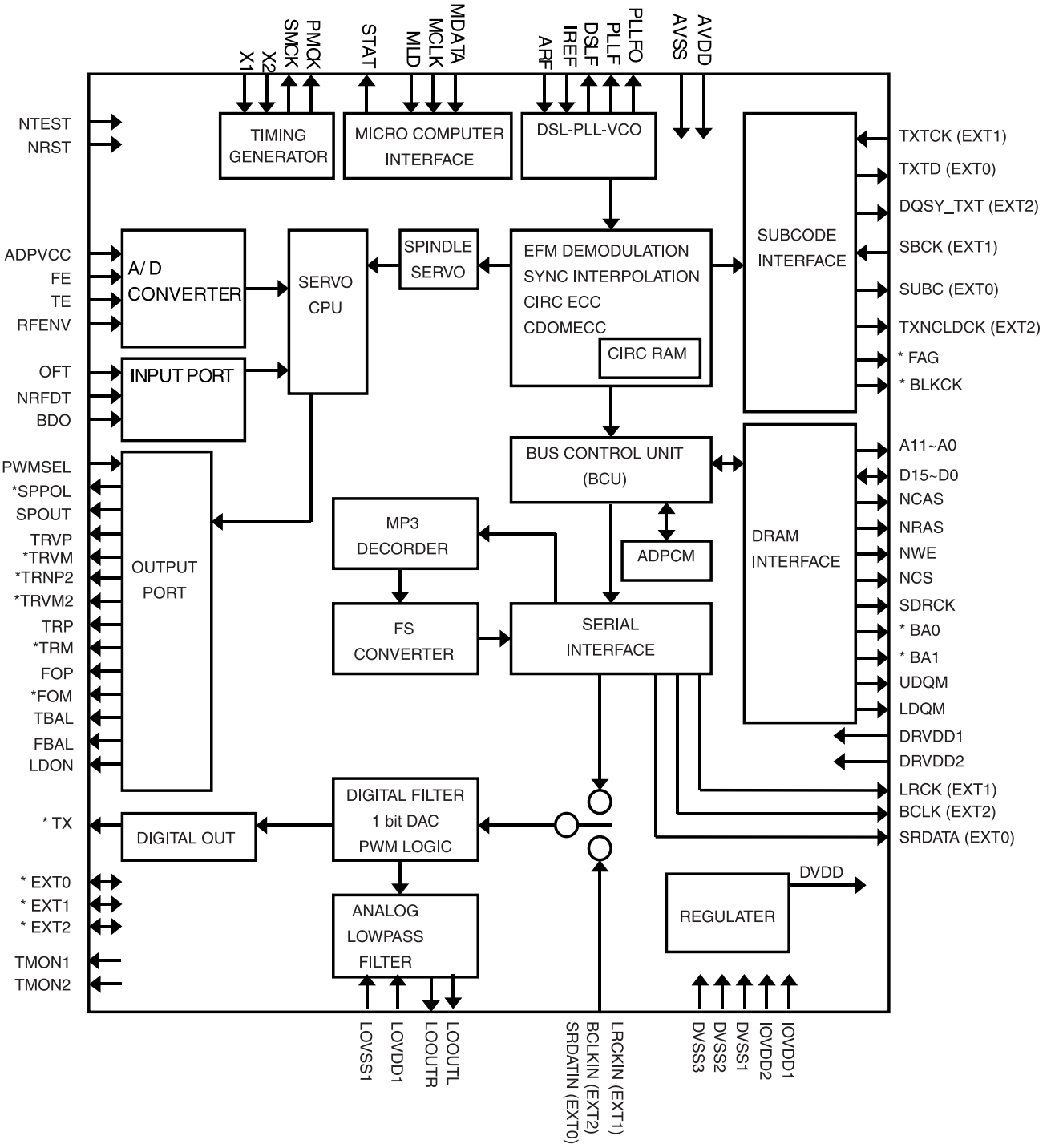
Pin	Name in Micom	Name in Model	I/O	Description
73	PC6/A6	PPWR_MUTE	O	To power amp, "MUTE" command output Mute(High), Sound(Low)
74	PC5/A5	PEV_CLK	O	Clock for interface with volume controller
75	PC4/A4	PEV_DO	O	To volume controller, data output
76	PC3/A3	PPWR	O	System Power supplier ON output On(High), Off(Low)
77	PC2/A2	PACC	I	From ISO jack, ACC signal input ACC On(Low), ACC Off(High)
78	PC1/A1	N.C	I	Not to be used
79	PC0/A0	PCDC_PWR	O	CD changer power supplier ON output CDC On(High), CDC Off(Low)
80	PA0/CS2#	PFRT_DET	I	Front pannel existence signal input Front Pannel Ok(High), Absent(Low)

■ IC501 MN6627933

1) PORT ASSIGNMENT



2) Block Diagram



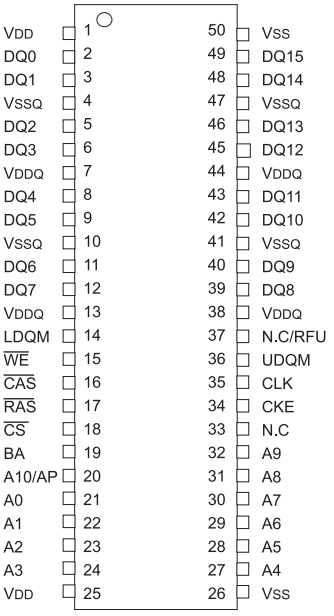
3) PORT DESCRIPTION

Pin No.	Symbol	I/O	Function
1	D11	I/O	DRAM data signal I/O 11
2	D10	I/O	DRAM data signal I/O 10
3	D9	I/O	DRAM data signal I/O 9
4	D8	I/O	DRAM data signal I/O 8
5	UDQM	O	SDRAM upper byte data mask signal output
6	SDRCK	O	SDRAM clock signal output
7	A11	O	DRAM address signal output 11
8	A9	O	DRAM address signal output 9
9	A8	O	DRAM address signal output 8
10	A7	O	DRAM address signal output 7
11	A6	O	DRAM address signal output 6
12	A5	O	DRAM address signal output 5
13	A4	O	DRAM address signal output 4
14	LDQM	O	SDRAM lower byte data mask signal output
15	NWE	O	DRAM write enable signal output
16	NCAS	O	DRAM CAS control signal output
17	NRAS	O	DRAM RAS control signal output
18	NCS	O	SDRAM chip select signal output
19	A3	O	DRAM address signal output 3
20	A2	O	DRAM address signal output 2
21	A1	O	DRAM address signal output 1
22	A0	O	DRAM address signal output 0
23	DRVDD1	I	Power supply 1 for DRAM interface I/O
24	DVSS1	I	Ground 1 for digital circuits
25	A10	O	DRAM address signal output 10
26	*BA1	O	SDRAM bank selection signal output 1
27	*BA0	O	SDRAM bank selection signal output 0
28	DVDD1	I	Power supply 1 for internal digital circuits
29	SPOUT	O	Spindle drive signal output (absolute value)
30	*SPPOL	O	Spindle drive signal output (polarity)
31	TRVP	O	Traverse drive signal output (positive polarity)
32	*TRVM	O	Traverse drive signal output (negative polarity)
33	*TRVP2	O	Traverse drive signal output 2 (positive polarity)
34	*TRVM2	O	Traverse drive signal output 2 (negative polarity)
35	TRP	O	Tracking drive signal output (positive polarity)
36	*TRM	O	Tracking drive signal output (negative polarity)
37	FOP	O	Focus drive signal output (positive polarity)
38	*FOM	O	Focus drive signal output (negative polarity)
39	IOVDD1	I	Power supply 1 for digital I/O
40	TBAL	O	Tracking balance adjustment signal output
41	FBAL	O	Focus balance adjustment signal output
42	FE	I	Focus error signal input
43	TE	I	Tracking error signal input
44	ADPVCC	I	Voltage input for supply voltage monitor
45	RFENV	I	RF envelope signal input
46	LDON	O	Laser ON signal output
47	NRFDET	I	RF detectoion signal input
48	OFT	I	Off-track signal input
49	BDO	I	Dropout signal input
50	AVDD1	I	Power supply 1 for analog circuits
51	IREF	I	Analog reference current input
52	ARF	I	RF signal input
53	DSLF	O	DSL loop filter pin
54	PWMSEL	I	PWM output mode selection input Low: Direct High: 3-state
55	PLLF	O	PLL loop filter pin (for phase comparison)
56	PLLFO	O	PLL loop filter pin (for speed comparison)
57	AVSS1	I	Ground 1 for analog circuits
58	LOOUTL	O	L-ch audio output for line-out output
59	LOVSS1	I	Ground for line-out output

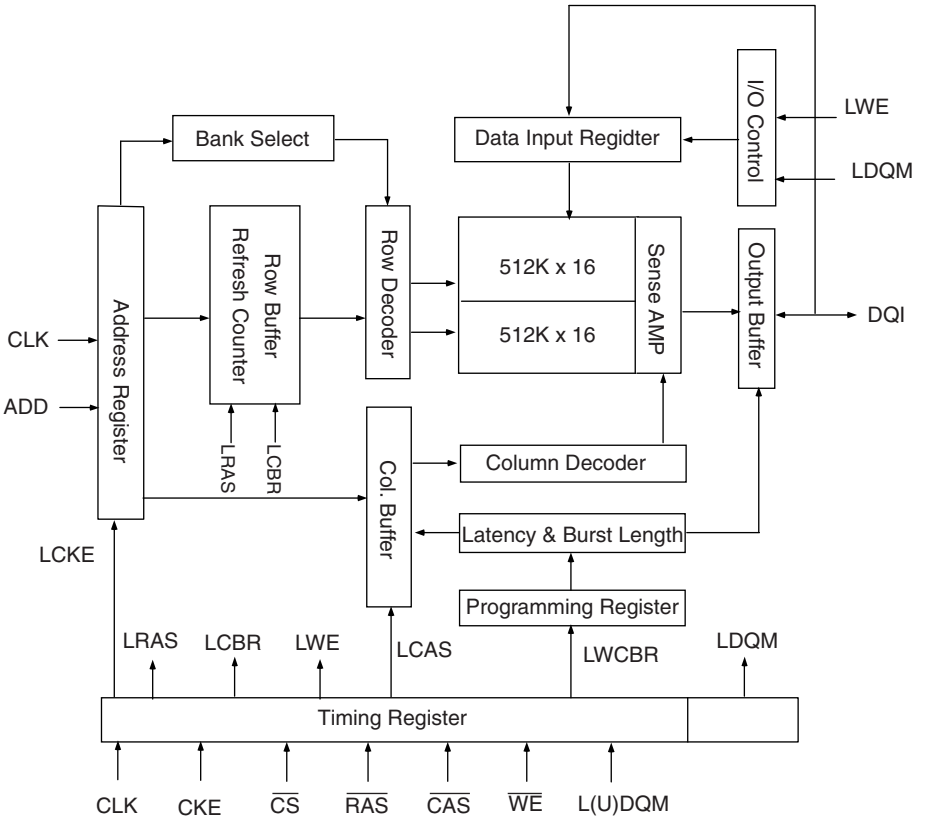
Pin No.	Symbol	I/O	Function
60	LOOUTR	O	R-ch audio output for line-out output
61	LOVDD1	I	Power supply for line-out output
62	N.C.	-	-
63	TMON1	O	Test monitor output 1
64	N.C.	-	-
65	N.C.	-	-
66	TMON2	O	Test monitor output 2
67	DVDD3	I	Power supply 3 for digital circuits
68	DVSS2	I	Ground 2 for digital circuits
69	*EXT0	I/O	Expansion I/O port 0
70	*EXT1	I/O	Expansion I/O port 1
71	*EXT2	I/O	Expansion I/O port 2
72	MCLK	I	Microcontroller command clock signal input
73	MDATA	I	Microcontroller command data signal input
74	MLD	I	Microcontroller command load signal input
75	*STAT	O	Status signal output
76	*BLKCK	O	Subcode block clock signal output
77	*SMCK	O	4.2336-/8.4672-MHz clock signal output
78	*PMCK	O	88.2-kHz clock signal output
79	*TX	O	Digital audio interface signal output
80	*FLAG	O	Flag signal output
81	NRST	I	LSI reset signal input
82	NTEST	I	Test mode setting input
83	DVSS3	I	Ground 3 for digital circuits
84	X1	I	Crystal oscillator circuit input
85	X2	O	Crystal oscillator circuit output
86	IOVDD2	I	Power supply 2 for digital I/O
87	DVDD2	I	Power supply 2 for internal digital circuits
88	D2	I/O	DRAM data signal I/O 2
89	D1	I/O	DRAM data signal I/O 1
90	D0	I/O	DRAM data signal I/O 0
91	D3	I/O	DRAM data signal I/O 3
92	D4	I/O	DRAM data signal I/O 4
93	D5	I/O	DRAM data signal I/O 5
94	D6	I/O	DRAM data signal I/O 6
95	D7	I/O	DRAM data signal I/O 7
96	D15	I/O	DRAM data signal I/O 15
97	D14	I/O	DRAM data signal I/O 14
98	DRVDD2	I	Power supply 2 for DRAM interface I/O
99	D13	I/O	DRAM data signal I/O 13
100	D12	I/O	DRAM data signal I/O 12

■ IC503 M12L16161A

1) PORT ASSIGNMENT



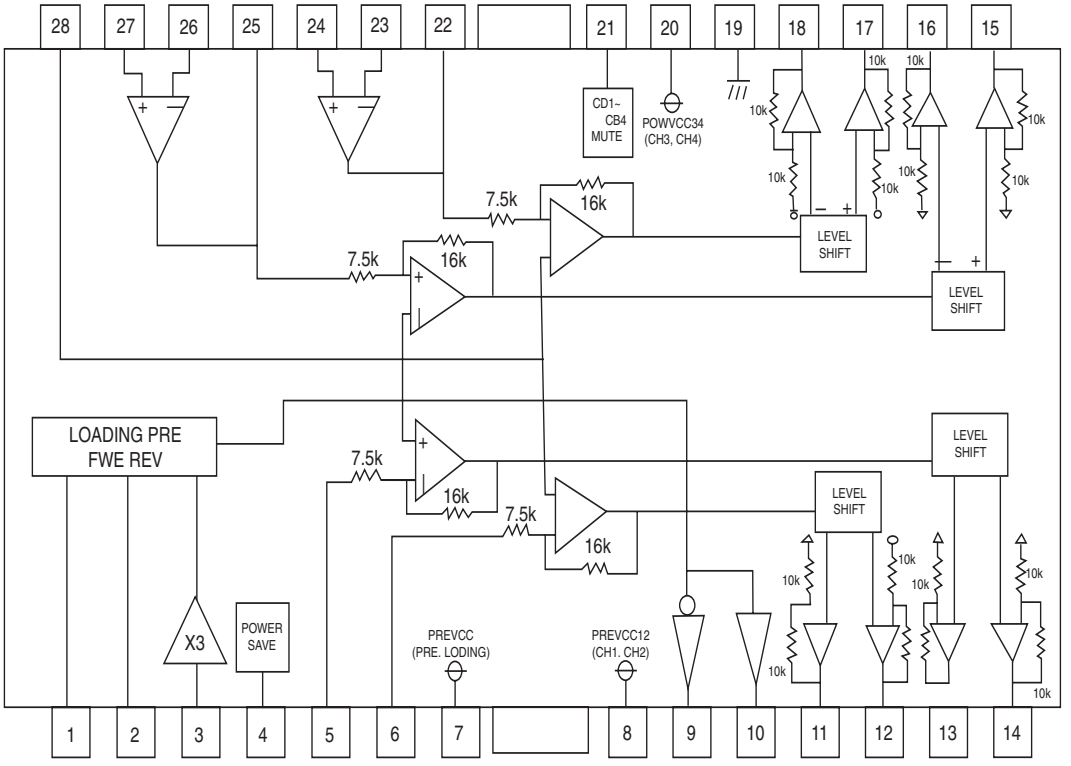
2) BLOCK DIAGRAM



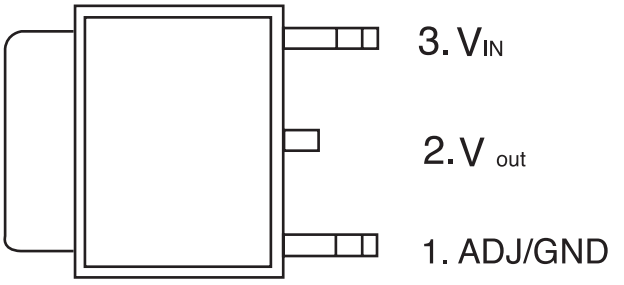
■ PIN Function table

Pin	Name	Input Function
CLK	System Clock	Active on the positive going edge to sample all inputs.
CS	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and L(U)DQM.
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0~A10/AP	Address	Row/Column addresses are multiplexed on the same pins. Row address: RA0~RA10, column address: CA0~CA7
BA	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
RAS	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with RAS low. Enables row access & precharge.
CAS	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with CAS low. Enables column access.
WE	Write Enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
L(U)DQM	Data Input / Output Mask	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0~15	Data Input / Output	Data inputs/outputs are multiplexed on the same pins.
VDD/VSS	Power Supply/Ground	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	Data Output Power/Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	No Connection/ Reserved for Future Use	This is recommended to be left No Connection on the device.

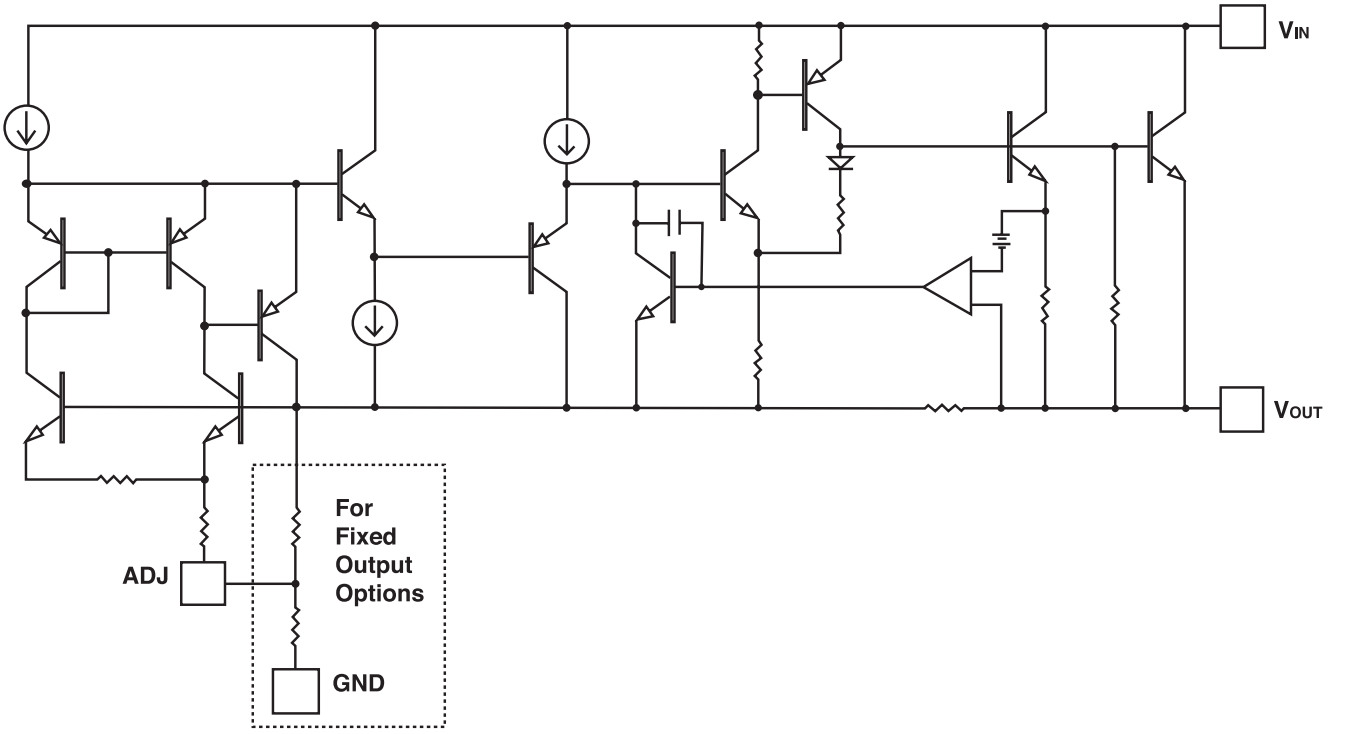
■ IC504 BA5810FM



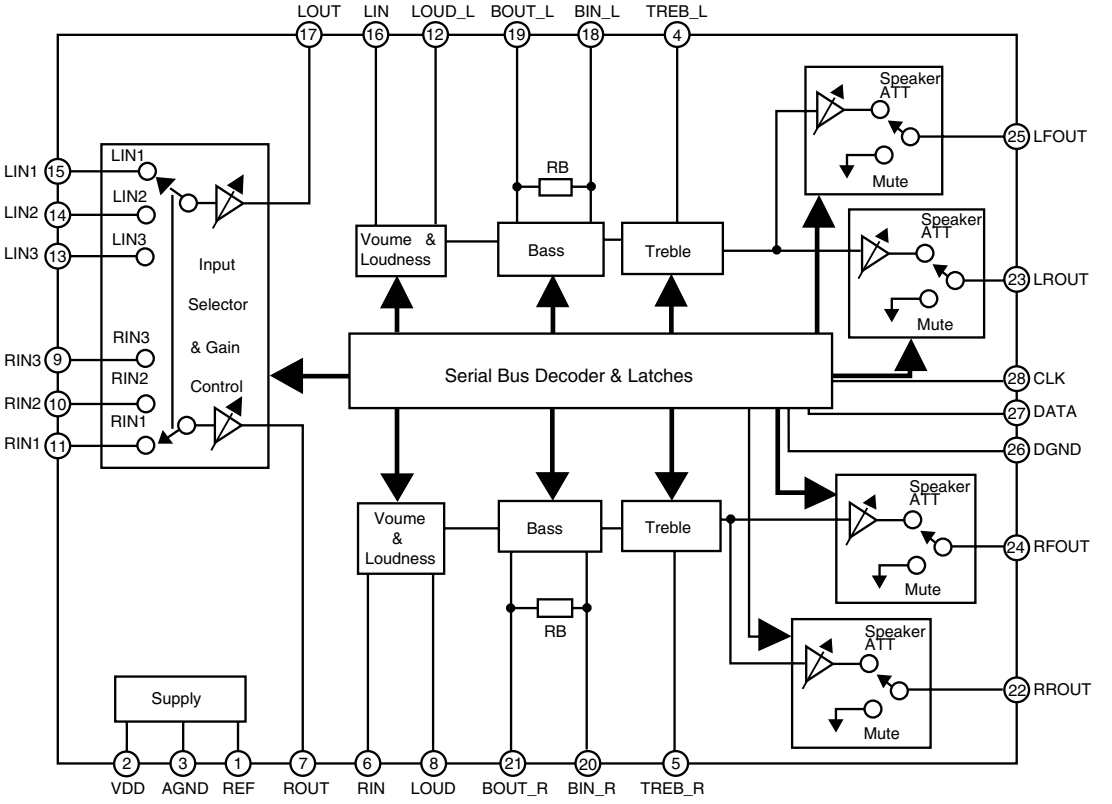
■ IC505 AMC1117



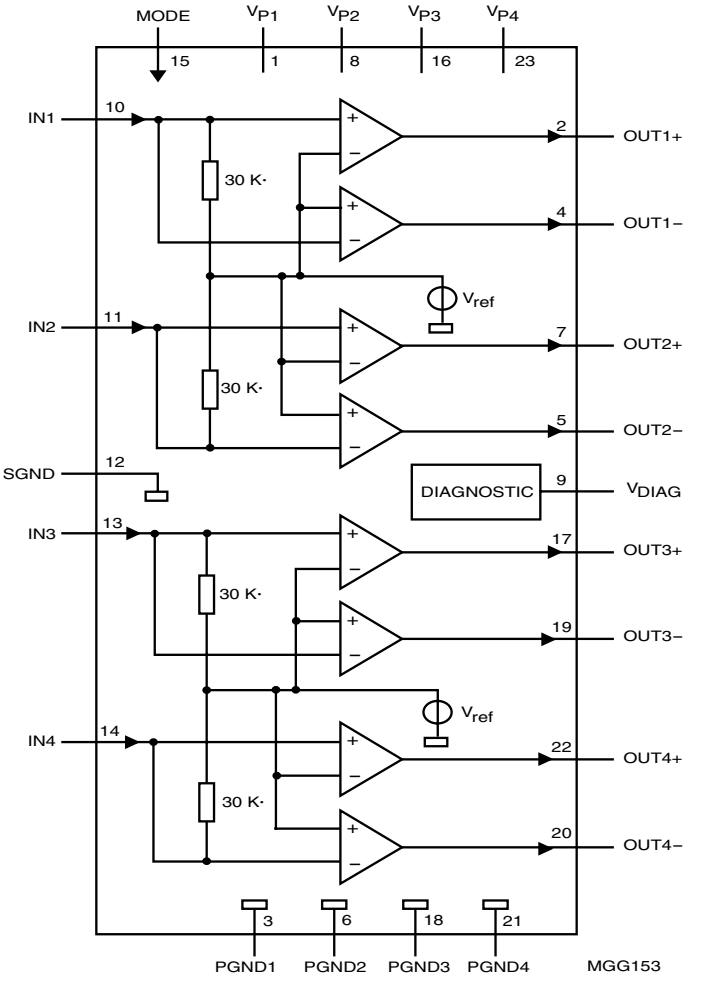
■ BLOCK DIAGRAM



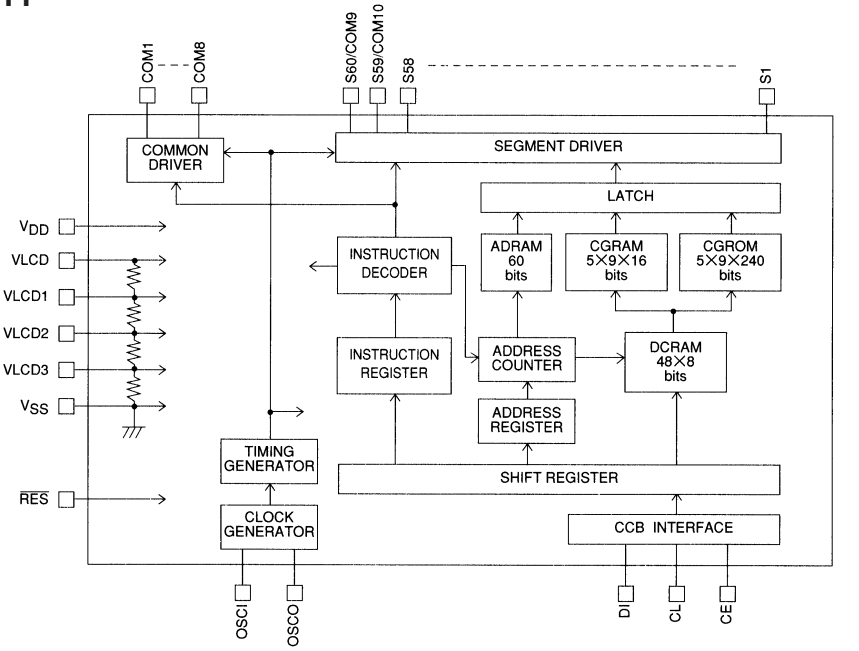
■ IC601 PT2313L



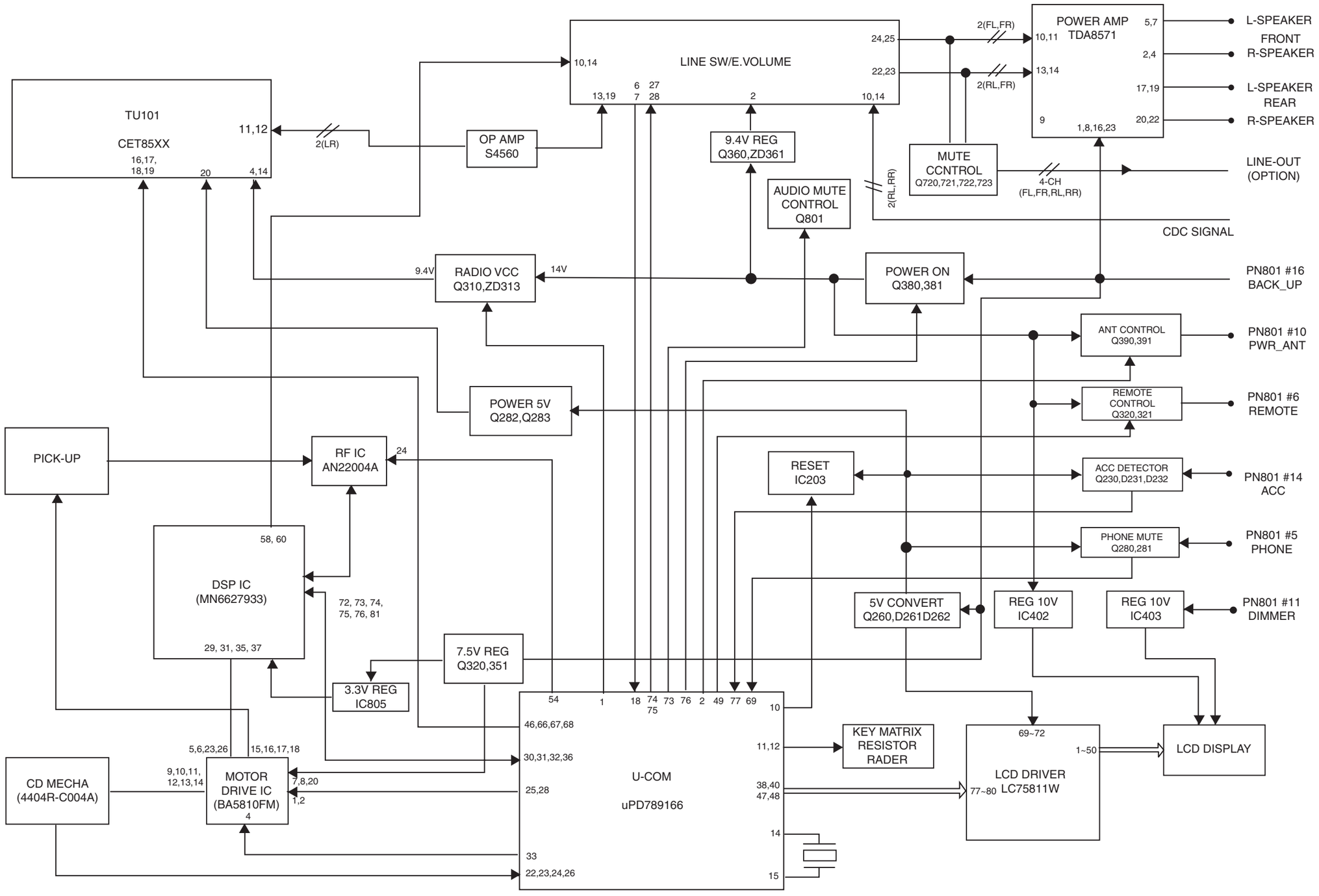
■ IC801 TDA8571J



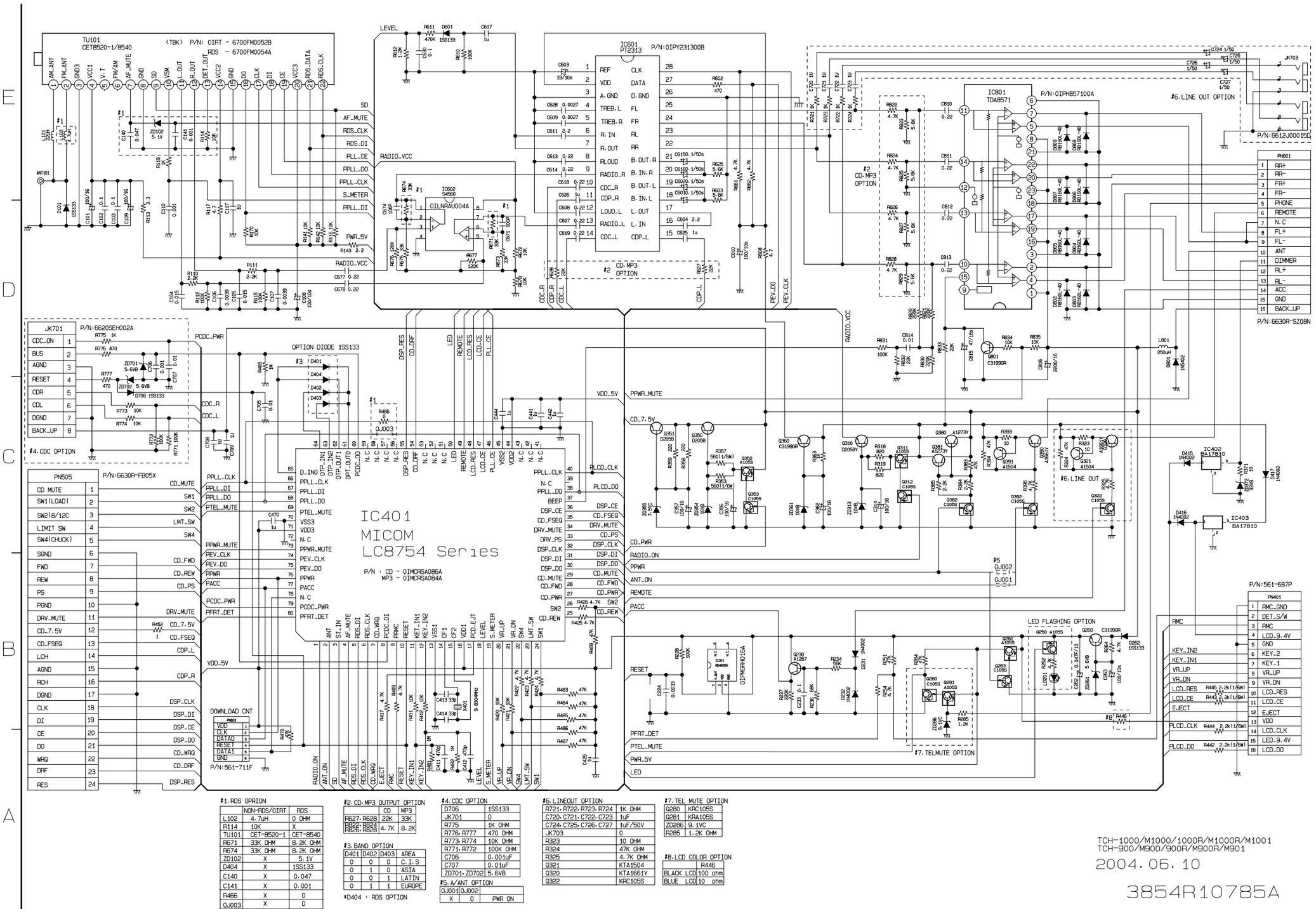
■ IC901 LC75811



❑ BLOCK DIAGRAM



❑ MAIN SCHEMATIC DIAGRAM



#1.RDS OPRION	NON-RDS/OIRT	RDS
L102	4.7uH	0 OHM
R114	10K	X
TU101	CET-8520-1	CET-8540
R671	33K OHM	8.2K OHM
R674	33K OHM	8.2K OHM
ZD102	X	5.1V
D404	X	1SS133
C140	X	0.047
C141	X	0.001
R466	X	0
OJ003	X	0

#2.CD.MP3 OUTPUT OPTION	CD	MP3
R627,R628	22K	33K
R629,R630	4.7K	8.2K

#3.BAND OPTION	D401	D402	D403	AREA
	0	0	0	C.I.S
	0	1	0	ASIA
	0	0	1	LATIN
	0	1	1	EUROPE

#4.CDC OPTION	
D706	1SS133
JK701	0
R775	1K OHM
R776,R777	470 OHM
R773,R774	10K OHM
R771,R772	100K OHM
C706	0.001uF
C707	0.01uF
ZD701,ZD702	5.6VB

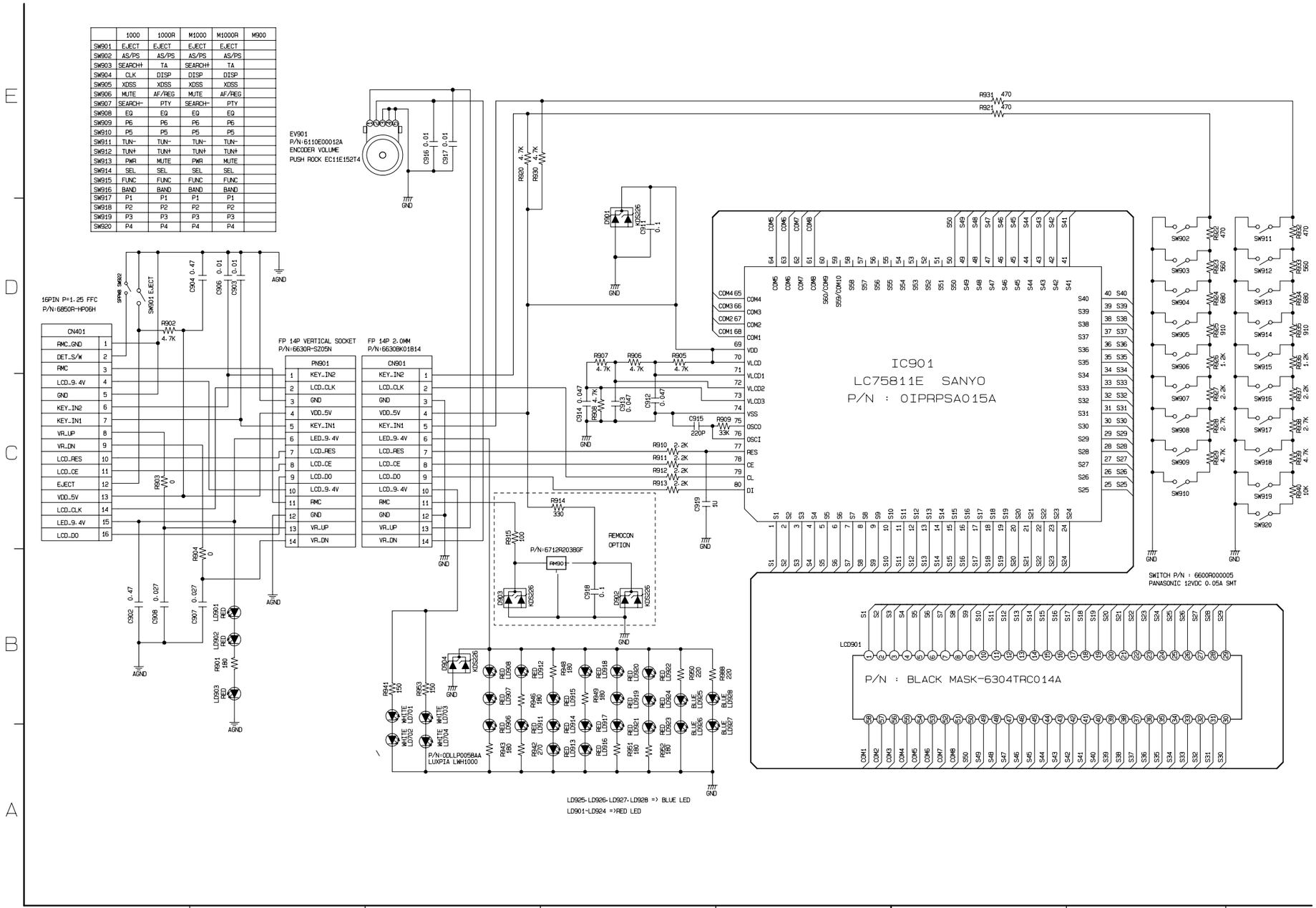
#5.A/ANT OPTION		
OJ001	OJ002	
X	0	PWR ON

#6.LINEOUT OPTION	
R721,R722,R723,R724	1K OHM
C720,C721,C722,C723	1uF
C724,C725,C726,C727	1uF/50V
JK703	0
R323	10 OHM
R324	47K OHM
R325	4.7K OHM
Q321	KTA1504
Q320	KTA1661Y
Q322	KRC105S

#7.TEL MUTE OPTION	
Q280	KRC105S
Q281	KRA105S
ZD286	9.1VC
R285	1.2K OHM

#8.LCD COLOR OPTION	R446
BLACK LCD	100 ohm
BLUE LCD	10 ohm

❑ FRONT SCHEMATIC DIAGRAM



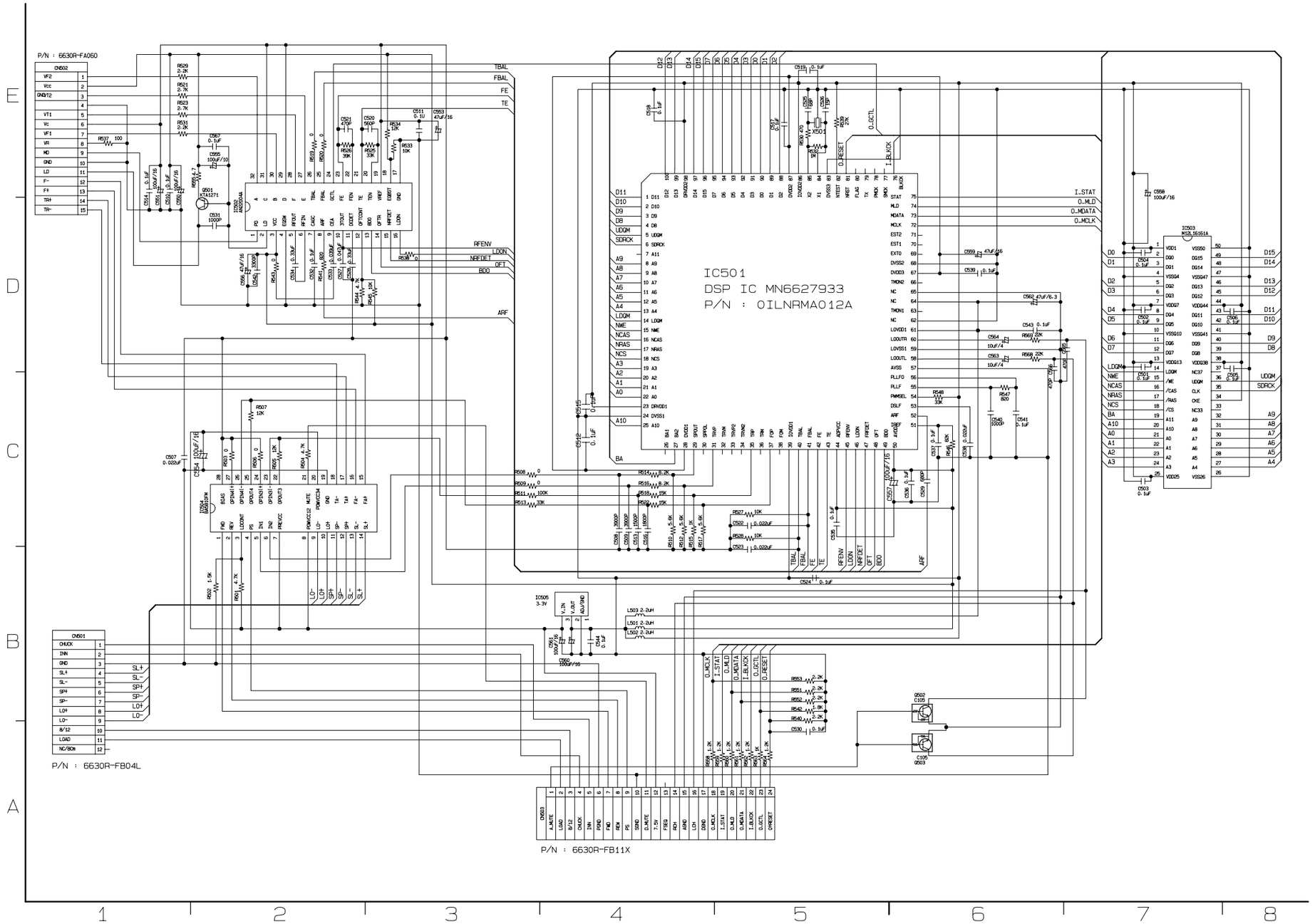
	1000	1000R	M1000	M1000R	M900
SW901	EJECT	EJECT	EJECT	EJECT	
SW902	AS/PS	AS/PS	AS/PS	AS/PS	
SW903	SEARCH+	TA	SEARCH+	TA	
SW904	CLK	DISP	DISP	DISP	
SW905	XDSS	XDSS	XDSS	XDSS	
SW906	MUTE	AF/REG	MUTE	AF/REG	
SW907	SEARCH-	PTY	SEARCH-	PTY	
SW908	EQ	EQ	EQ	EQ	
SW909	P6	P6	P6	P6	
SW910	P5	P5	P5	P5	
SW911	TUN-	TUN-	TUN-	TUN-	
SW912	TUN+	TUN+	TUN+	TUN+	
SW913	PWR	MUTE	PWR	MUTE	
SW914	SEL	SEL	SEL	SEL	
SW915	FUNC	FUNC	FUNC	FUNC	
SW916	BAND	BAND	BAND	BAND	
SW917	P1	P1	P1	P1	
SW918	P2	P2	P2	P2	
SW919	P3	P3	P3	P3	
SW920	P4	P4	P4	P4	

CN401	
RMC_GND	1
DET_S/W	2
RMC	3
LCD_9.4V	4
GND	5
KEY_IN2	6
KEY_IN1	7
VR_UP	8
VR_DN	9
LCD_RES	10
LCD_CE	11
EJECT	12
VDD_5V	13
LCD_CLK	14
LED_9.4V	15
LCD_DO	16

PN901	
KEY_IN2	1
LCD_CLK	2
GND	3
VDD_5V	4
KEY_IN1	5
LED_9.4V	6
LCD_RES	7
LCD_CE	8
LCD_DO	9
LCD_9.4V	10
RMC	11
GND	12
VR_UP	13
VR_DN	14

CN901	
KEY_IN2	1
LCD_CLK	2
GND	3
VDD_5V	4
KEY_IN1	5
LED_9.4V	6
LCD_RES	7
LCD_CE	8
LCD_DO	9
LCD_9.4V	10
RMC	11
GND	12
VR_UP	13
VR_DN	14

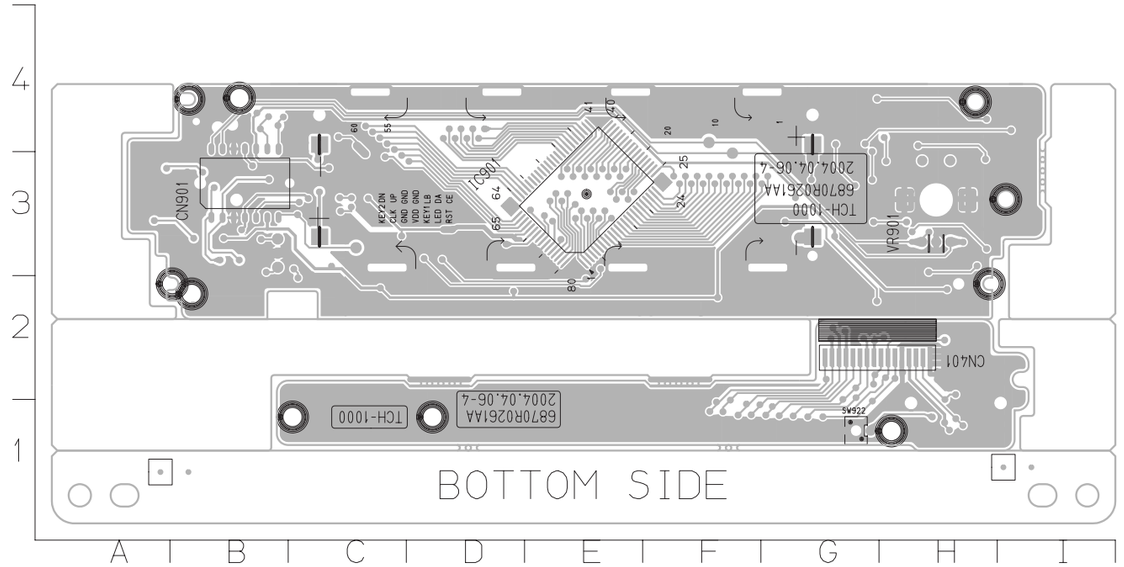
❑ CDP SCHEMATIC DIAGRAM



❑ PRINTED CIRCUIT DIAGRAM

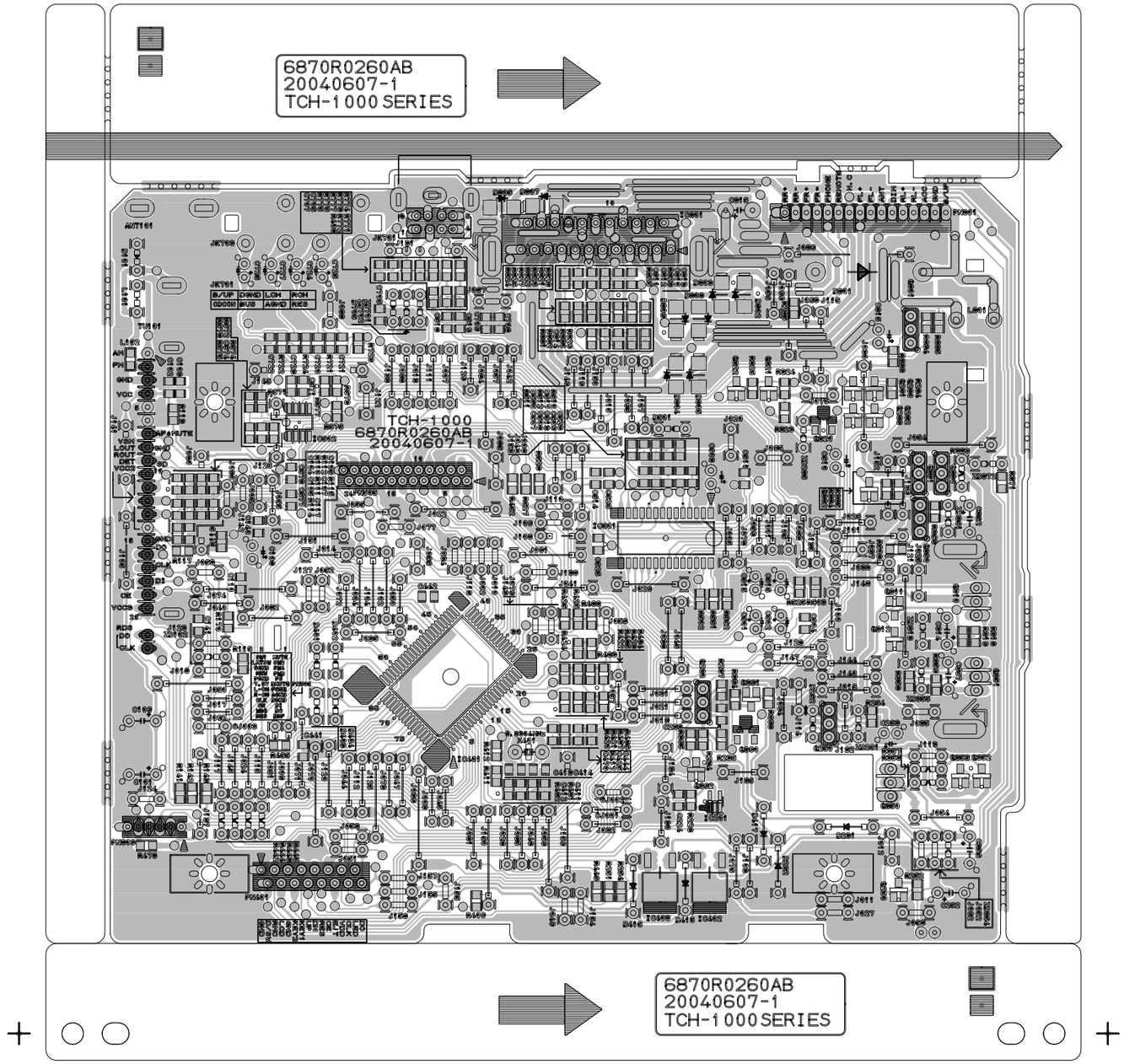
1. LED P.C.BOARD (COMPONENT SIDE)

2. FRONT P.C. BOARD (COMPONENT SIDE)

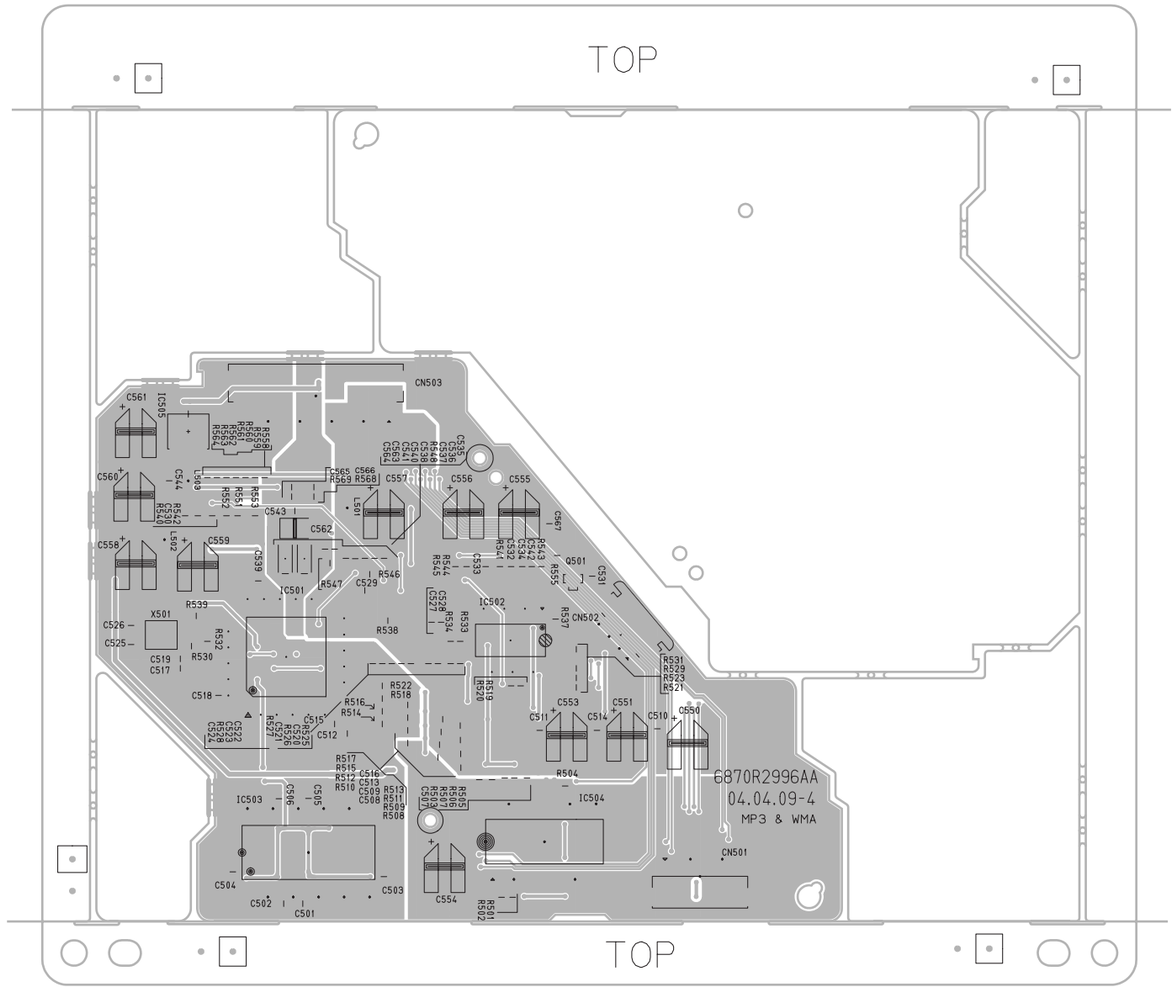


C901	G1	LD920	B3	R935	G4
C902	F1	LD921	B3	R936	G2
C903	G1	LD922	B3	R937	G2
C904	F1	LD923	B3	R938	F2
C905	F1	LD924	B3	R939	F2
C906	G1	LD925	H3	R940	E2
C907	G2	LD926	I3	R941	C3
C908	G2	LD927	I3	R942	G2
C909	F1	LD928	H3	R943	I4
C910	G1	PN901	H1	R946	F2
C911	H3	R901	D1	R948	E2
C912	H4	R902	G1	R949	D2
C913	H4	R903	G2	R950	H2
C914	H4	R904	H2	R951	B4
C915	E2	R905	H4	R952	A3
C916	H3	R906	H4	R953	G3
C917	H3	R907	H4	R988	H2
C918	B2	R908	H4	RM901	B3
C919	B4	R909	E2	SW901	C1
CN401	H2	R910	B3	SW902	B3
D901	H3	R911	B4	SW903	B3
D902	B2	R912	B3	SW904	A3
D903	B2	R913	B4	SW905	A3
D904	H2	R914	B2	SW906	B4
LCD901	G4	R915	B2	SW907	B3
LD901	F1	R920	B3	SW908	C2
LD902	E1	R921	B3	SW909	D2
LD903	C1	R922	B3	SW910	D2
LD906	I4	R923	B3	SW911	I3
LD907	G4	R924	A3	SW912	I3
LD908	G3	R925	B3	SW913	I4
LD911	G2	R926	B3	SW914	G4
LD912	F2	R927	C2	SW915	G3
LD913	F2	R928	C2	SW916	G2
LD914	E2	R929	D2	SW917	F2
LD915	E2	R930	H2	SW918	F2
LD916	D2	R931	H2	SW919	E2
LD917	D2	R932	H3	SW920	E2
LD918	C2	R933	H3	SW922	G1
LD919	B3	R934	G4	VR901	H3

3. MAIN P.C. BOARD
(SOLDER SIDE)



4. CDP P.C. BOARD(COMPONENT SIDE)



MEMO

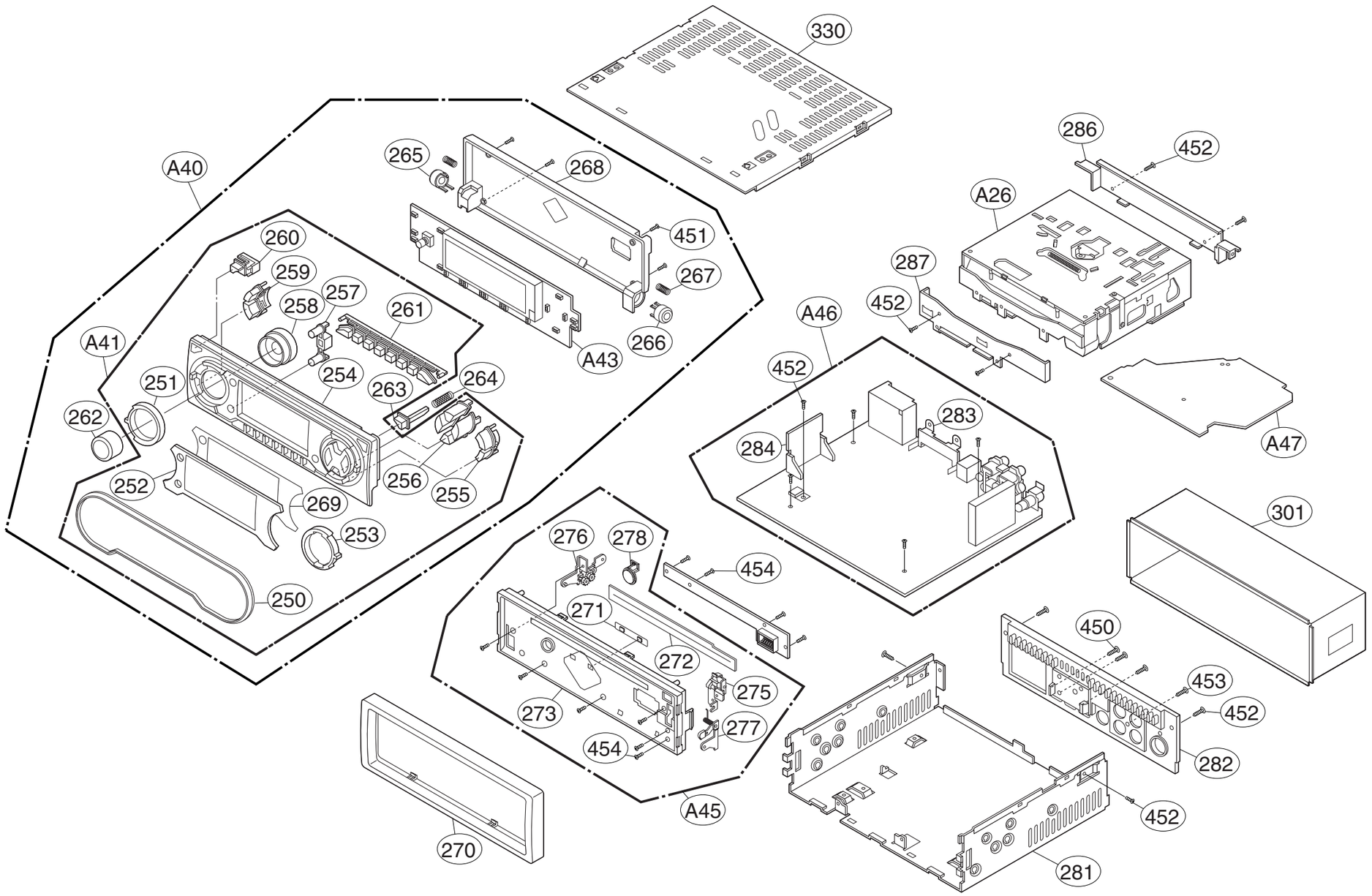
MEMO

SECTION 3. CABINET MAIN CHASSIS & MECHANISM

■ EXPLODED VIEW

NOTE) Refer to "SECTION 4 REPLACEMENT PARTS LIST" in order to look for the part number of each part.

⚠ CAUTION
Exposed blade will cause severe injury



MEMO

MEMO