MB81 IDTV
SERVICE MANUAL

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1. INTRODUCTION

17MB81 mainboard is driven by MediaTek MT5356. This IC is capable of handling Video and audio processing, Scaling-Display processing, 3D comb filter, OSD and text processing, LVDS/mini-LVDS transmitting, channel and MPEG2/4 decoding, integrated DVB-T/C demodulator and media center functionality.

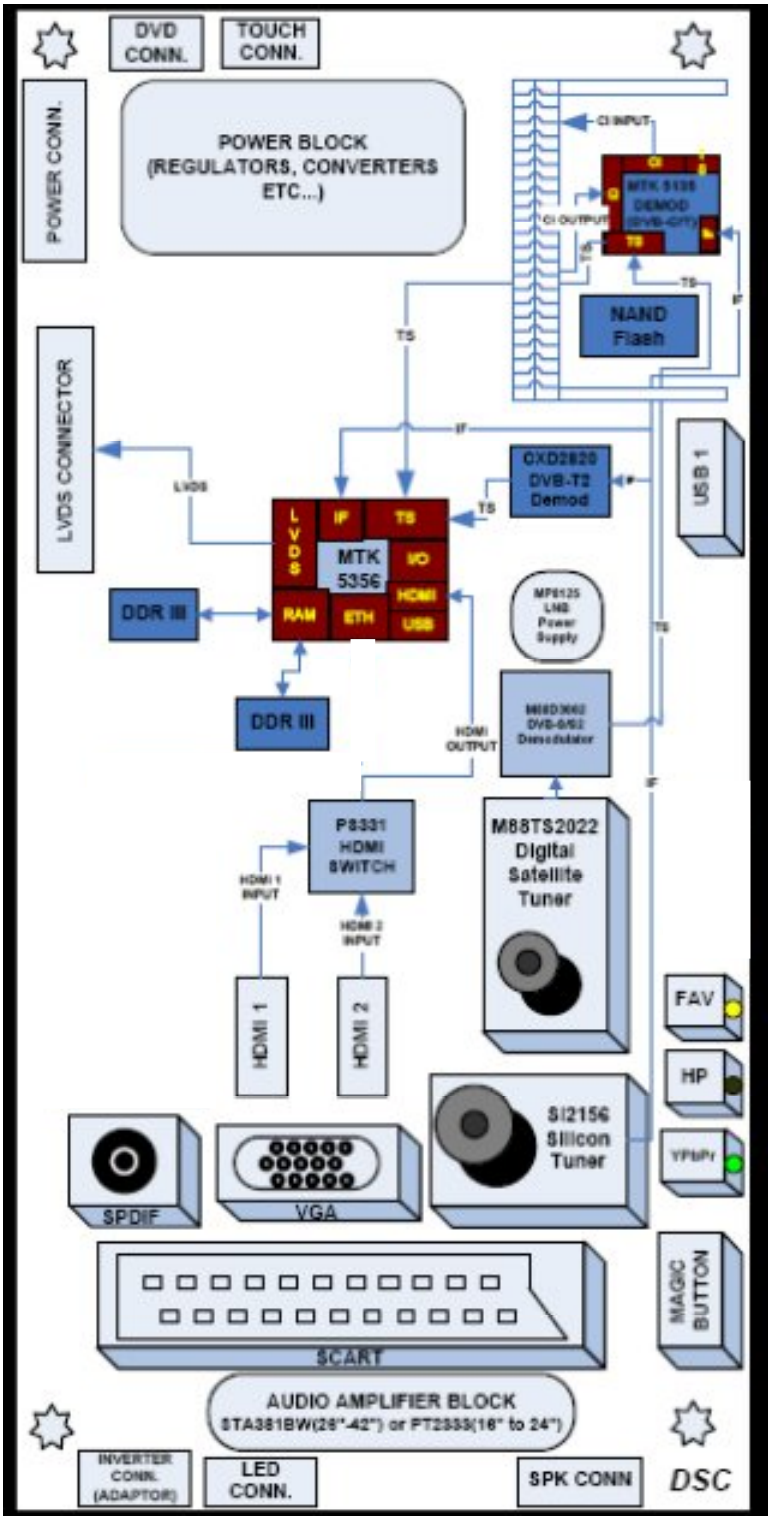
TV supports PAL, SECAM, NTSC colour standards and multiple transmission standards as B/G, D/K, I/I', and L/L' including German and NICAM stereo. Also DVB T, DVB-C are supported internal demoulators of MediaTek IC and DVB-S/S2 is supported with externall demodulator.

Sound system output is supplying max. 2x8W (less 10%THD at max output) for stereo 8Ω speakers.

Supported peripherals are:

1 RF input VHF I, VHF III, UHF @ 75Ohm(Common)
1 Side AV (CVBS, R/L_Audio)
1 SCART socket(Common)
1 YPbPr (Optional)
1 PC input(Common)
2 HDMI 1.3 input(1 HDMI input is common, 1 input is optional)
1 S/PDIF output(Optional)
1 Headphone(Optional)
1 Common interface(Common)
1 USB input is (Common)
1 On-board Keypad(Optional)
1 External Keypad(Optional)
1 External TouchPad(Optional)

1.1. General Block Diagram



1.2. MB81 Placement of Blocks

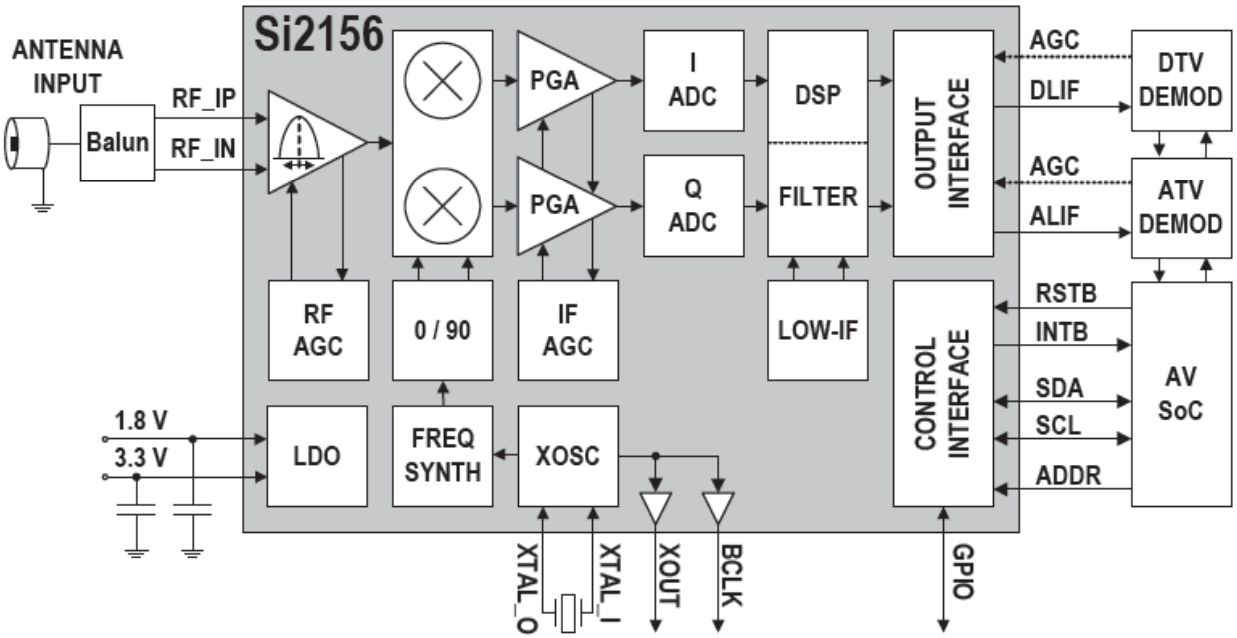
1. TUNER(Sİ2156)

The Si2156 integrates a complete hybrid TV tuner supporting all worldwide terrestrial and cable TV standards. Leveraging Silicon Labs' field proven third generation digital low-IF architecture, the Si2156 maintains the unmatched performance and design simplicity of the original Si2153 while further reducing footprint size. No external LNAs, tracking filters, or SAW filters are used. Compared with competing silicon tuners and discrete MOPLL-based tuners, the Si2156 delivers superior picture quality and a higher number of received stations in real-world conditions due to its very high linearity and low noise. Interfacing the Si2156 seamlessly with the Si2165 DVB-T/C demodulator creates a DVB-T/C receiver plus PAL/SECAM tuner. The Si2156 is pin-compatible with the Si2176 hybrid TV tuner with analog demodulator, providing customers unparalleled design flexibility.

Features :

- Worldwide hybrid TV tuner
  - Analog TV: NTSC, PAL/SECAM
  - Digital TV: ATSC/QAM, DVB-T/T2/C, ISDB-T/C, DTMB
  - 42–1002 MHz frequency range
- Compliance with A/74, NorDig, D-Book, C-Book, ARIB, EN55020, OpenCable™ specifications
- Highly-integrated, lowest BOM
  - No SAW filters required
  - Integrated LNA and tracking filters
- No alignment, tuning or calibration
- Best-in-class real-world reception
  - Exceeds MOPLL-based tuners
- Digital low-IF architecture
  - Customizable channel select filter
- Flexible output interface
  - Single or separate pins for ALIF/DLIF connection to SoC
- 3.3 and 1.8 V supply voltage
- Standard CMOS process
- 5 x 5 mm, 32-pin QFN package
- RoHS compliant

BLOCK DIADRAM



M88TS2022 (Optional)

Features

- Single-chip tuner
- Compliant with DVB-S2 and ABS-S standards
- Support QPSK, 8PSK and 16APSK
- Direct-conversion from L-band to baseband
- Symbol rate: 1 to 45 Msymbol/s
- Integrated VCOs and PLL, with on-chip inductors, varactors and loop filter
- Integrated baseband filters: 4 MHz to 40 MHz bandwidth
- Integrated RF AGC for optimal performance
- Integrated baseband DC offset cancellation (patent-pending) removes external loop filters
- Excellent immunity to strong adjacent undesired channels
- Integrated clock driver provides auxiliary divided clock output for other devices
- Selectable RF bypass
- Support sleep mode
- 2-wire serial bus with 3.3 V compatible logic levels
- Power supply: +3.3 V
- 28-pin QFN (Quad Flat No-lead) package
- RoHS compliant

Applications

- Digital satellite receiver front-end for DVB-S2 and ABS-S applications

General Description

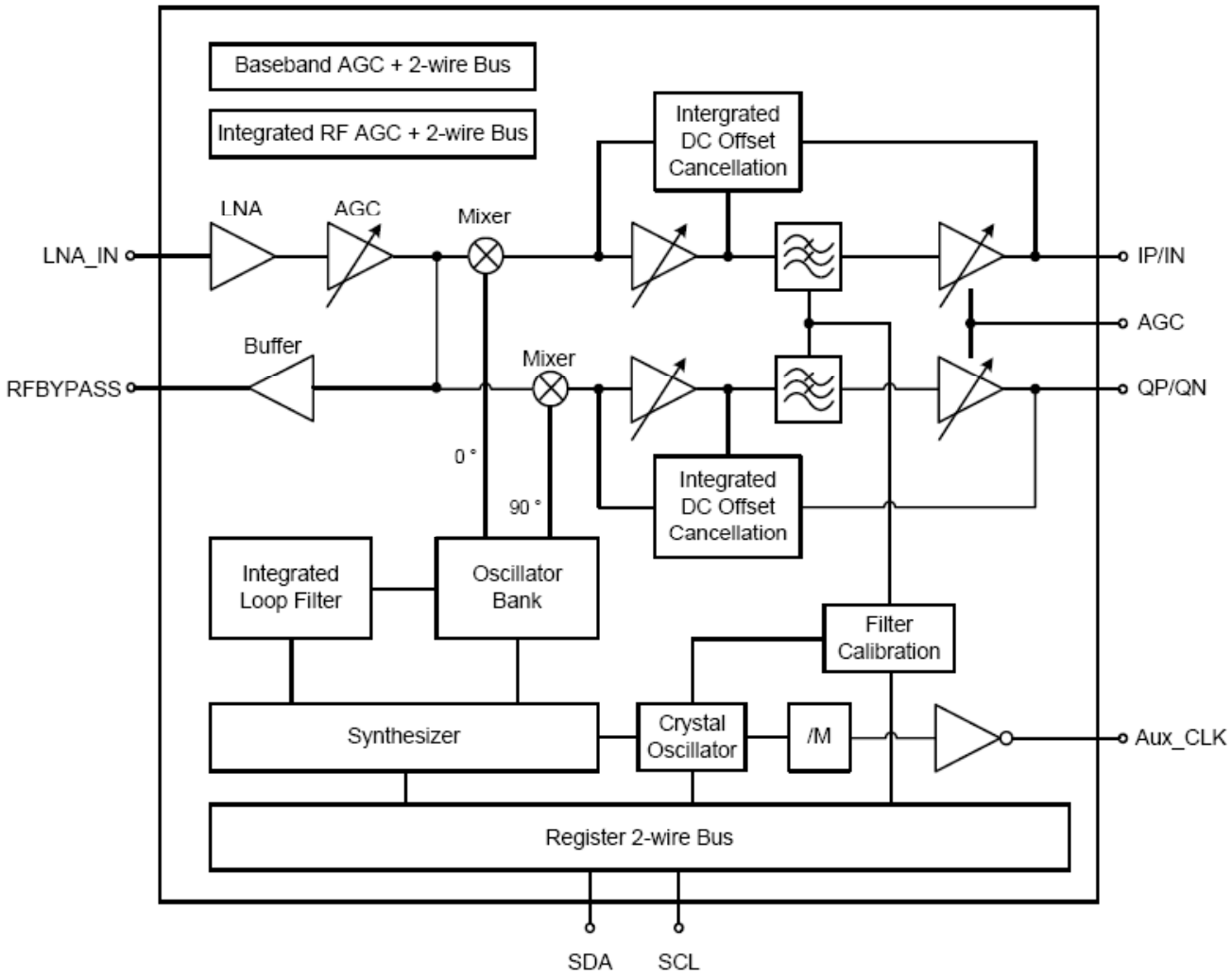
The M88TS2022 is a single-chip, direct-conversion tuner for digital satellite receiver applications. It offers the industry's most integrated solution to a satellite tuner function, simplifying the front-end designs. The device also provides an RF bypass output for driving a second tuner module.

This device incorporates the following functional blocks on a single chip: an LNA, quadrature down-converting mixers, a low phase noise and fast locking frequency synthesizer with on-chip loop filters, a DC offset cancellation loop with integrated loop filters, self-calibrated programmable baseband channel filters, an integrated RF AGC loop, and crystal oscillators with an integrated auxiliary clock output.

As a result of integrating all these blocks, the M88TS2022 has the least number of pins compared with other conventional solutions, and requires the least external components. In typical applications, the M88TS2022 requires only one crystal, one bypass capacitor, one matching network, and a few external resistors. The device also has the industry's smallest latency, as it uses a fast locking PLL and a fast settling DC offset cancellation architecture.

The M88TS2022 can be configured via a 2-wire serial bus. The chip is available in a 28-pin QFN package.

Block Diagram



M88DS3002 (Optional)

Features

- **Multi-standard demodulation**
  - Compliant with DVB-S/S2 specification
  - QPSK, 8PSK, 16APSK and 32APSK demodulation schemes
  - Maximum channel bit rate is 130 Mbps
  - Maximum symbol rates are: 45 Msps for QPSK and 8PSK; 36 Msps for 16APSK and 28 Msps for 32APSK
- **DSP features**
  - Symbol rate sweeping
  - I/Q impairment cancellation
  - Automatic spectrum inversion
  - Adaptive equalizer for RF reflection removal
  - Roll-off factor automatic identification
  - Blind scan for programming search
  - High performance on-chip micro-controller
  - Multi-error monitor
  - Accurate SNR estimation
  - Multi-lock indicators
  - Clipping rate reporter
  - DC removal
  - Automatic frequency correction (AFC)
  - Fast timing loop acquisition
  - Robust frame synchronization scheme
  - Phase noise indicator
  - Fast system recovery from fading or other abnormal conditions
  - Co-channel interference cancellation
  - Constellation monitor
- **Interface**
  - DVB-S/S2 common, parallel and serial MPEG output interface compliant
  - 2-wire serial bus to configure the device
  - 2-wire bus repeater for tuner configuration
  - DiSEqC™ 2.X compliant interface
  - General purpose output (GPO)
  - Dedicated reference clocks (13.5MHz / 27MHz) generation
- **System**
  - On-chip 8-bit ADC
  - On-chip PLL for master clock from a 27 MHz external clock or quartz crystal
  - Sleep mode supported
- **Technology**
  - Power supplies: 1.25 V and 3.3 V
  - Low power consumption: ~390 mW
  - Package: 64-pin QFN
  - RoHS compliant

Applications

- Digital satellite set-top boxes
- Digital satellite receivers

General Description

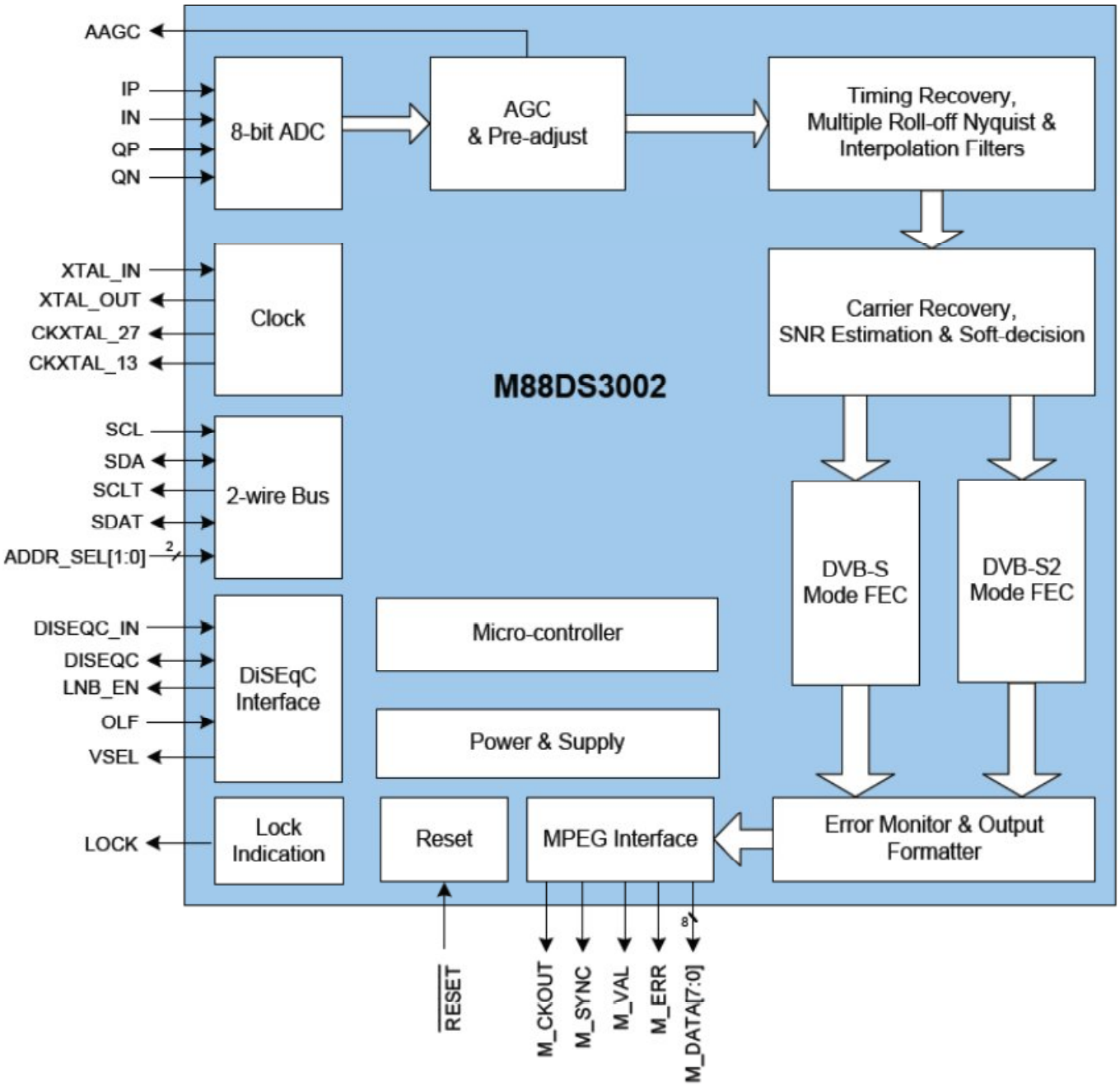
The M88DS3002 is an advanced single-chip demodulator for digital satellite television broadcasting. It is fully compliant with the DVB-S/S2 standard and can support QPSK, 8PSK, 16APSK and 32APSK demodulation schemes. The chip provides a fast, easy-to-apply and cost-effective front-end solution for digital satellite receiver.

The M88DS3002 accepts baseband differential or single-ended I and Q signals from a tuner, then digitizes, demodulates and decodes the signals, and finally outputs an MPEG transport stream.

The M88DS3002 supports symbol rate from 1 Msps up to 45 Msps, and code rate from 1/4 to 9/10. Its features cover blind scan, fade detection, timing and carrier recovery, performance monitoring, co-channel interference cancellation, command interface, and DiSEqC™ 2.X interface, etc. The device is controlled via a 2-wire serial bus.

The M88DS3002 works properly with 1.25 V and 3.3 V voltage supplies. Typically, the power consumption is around 390 mW. The chip is available in a 64-pin QFN package and is RoHS compliant.

Block Diagram



2. AUDIO AMPLIFIER STAGE

STA381BWS

2.1. General Description

The STA381BWS is an integrated solution embedding digital audio processing, digital amplification, FFXTM power output stage, headphone and 2 Vrms line outputs. It is part of the Sound Terminal® family and provides full digital audio streaming from the source to the speaker, offering cost effectiveness, low power dissipation and sound enrichment.
The STA381BWS input section consists of a flexible digital input serial audio interface, feeding the digital processing unit, and an analog 1 Vrms input for a seamless connection with pure analog sources. The serial audio data input interface supports many formats, including the popular IIS format.

The STA381BWS is based on an FFXTM (Fully Flexible Amplification) processor, an STMicroelectronics proprietary technology. FFXTM is the evolution of the ST ternary technology: the advanced processor is available for ternary, binary, binary differential and phase shift PWM modulation. STA381BWS embeds the ternary, binary and binary differential implementations, a subset of the full capability of the FFXTM processor.
The STA381BWS power section consists of four independent half-bridges. These can be configured via digital control to operate in different modes. A 2.1 channel setup can be implemented with two half-bridges (L/R) together with a single full-bridge (subwoofer).
Alternatively, the 2.0 channel setup can be done with two full-bridges. When using this configuration an external amplifier, for the SW channel, can be also driven through the PWM output. The STA381BWS is able to deliver 2 x 20 W (ternary) into an 8 W load at 18 V or 2 x 9 W (binary) into a 4 W load plus 1 x 20 W (ternary) into an 8 W load at 18 V. The STA381BWS also provides a capless headphone out (with embedded negative charge pump), able to deliver up to 40 mW into a 32 W load or, alternatively, can be configured as a 2 Vrms line output.

The STA381BWS digital processing unit includes up to 12 programmable biquads (EQs) allowing perfect sound equalization and offering advanced noise-shaping techniques.
Moreover, the coefficient range ensures a great variety of filter shapes (low/high-pass, low/high shelf, peak, notch, band-pass). The equalization engine is fully compatible with the ST speaker compensation technology embedded into the APWorkbench suite. A state-ofthe- art multi-band DRC, STCompressorTM, equalizes the system to provide active speaker protection with full audio quality preservation against sudden sound peaks. Moreover, STSpeakerSafeTM technology offers reliable speaker protection under any condition. The master clock can be from stable BICKI (64xfs, 50% duty cycle) or external XTI.

2.2. Features

Features
● Wide-range supply voltage
– 4.5 V to 25.5 V (operating range)
– 27 V (absolute maximum rating)
● I2C control with selectable device address
● Full IC protection embedding:
– Manufacturing short-circuit protection (out
vs. gnd, out vs. vcc, out vs. out)
– Thermal protection
– Overcurrent protection
– Undervoltage protection

● 1 Vrms stereo analog input
● I2S interface, sampling rate 32 kHz ~ 192 kHz, with internal sampling frequency converter for fixed processing frequency
● Three output power stage configurations
– 2.0 mode, L/R full bridges
– 2.1 mode, L/R two half-bridges, subwoofer full bridge
– 2.1 mode, L/R full bridges, PWM output for external subwoofer amplifier
● Driving load capabilities
– 2 x 20 W into 8 W ternary modulation
– 2 x 9 W into 4 W + 1 x 20 W into 8 W
● FFXTM 100 dB dynamic range
● Fixed output PWM frequency at any input sampling frequency
● Embedded RMS meter for measuring real-time loudness
● Two analog outputs:
– Selectable headphone / line out driver with adjustable gain via external resistors
– Auxiliary F3XTM analog output for external driver
● Headphone:
– Embedded negative charge pump
– Full capless output configuration
– Driving load capabilities: 40 mW into 32 W
● Line out:
– 2 Vrms line output capability
● Up to 12 user-programmable biquads with noise-shaping technology
● Direct access to coefficients through I2C shadowing mechanism
● Fixed (88.2 kHz / 96 kHz) internal processing sampling rate
● Two independent DRCs configurable as a dual-band anticlipper or independent limiters/compressors (B2DRC)
● Digital gain/att +48 dB to -80 dB with 0.125 dB/step resolution
● Independent (fade in, fade out) soft volume update with programmable rate 48 ~ 1.5 dB/ms
● Bass/treble tones control
● Audio presets:15 crossover filters, 5 anticlipping modes, nighttime listening mode
● STSpeakerSafeTM protection circuitry:
– Pre and post processing DC blocking filters
– Checksum engine for filter coefficients
– PWM fault self-diagnosis
● STCompressorTM dual-band DRC

2.3. Absolute Ratings

2.3.1. Electrical Characteristics

The specifications given in this section are valid for the operating conditions: V_{CC} = 18 V, f = 1 kHz, f_{sw} = 384 kHz, T_{amb} = 25°C and R_L = 8 Ω, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Po	Output power BTL	Digital limited(3)		20		W
	Output power SE	Digital limited(3)		5		
	Output power SE R_L = 4 Ω	Digital limited(3)		9		
R_{dsON}	Power Pchannel/Nchannel MOSFET	I_d = 1.5 A		120		mΩ
gP	Power Pchannel R_{dsON} matching	I_d = 1.5 A	95			%
gN	Power Nchannel R_{dsON} matching	I_d = 1.5 A	95			%
Idss	Power Pchannel/Nchannel leakage				10	µA
I_{LDT}	Low current dead time (static)	Resistive load(1)		8	15	ns
t_r	Rise time	Resistive load(1)		10	18	ns
t_f	Fall time	Resistive load(1)		10	18	ns
I_{vcc}	Supply current from Vcc in power-down	PWRDN = 0		0.1	1	µA
	Supply current from Vcc in operation	PCM Input signal = -60 dBfs, Switching frequency = 384 kHz, No LC filters		52	60	mA
Ilim	Overcurrent limit	(2)	4	5	6.5	A
UVL	Undervoltage protection			3.5	4.3	V
t_{min}	Output minimum pulse width	No load	20	30	60	ns
DR	Dynamic range			100		dB
SNR	Signal to noise ratio, ternary mode	A-Weighted		100		dB
	Signal to noise ratio binary mode	A-Weighted		90		dB
THD+N	Total harmonic distortion + noise	FFX stereo mode, Po = 1 W, f = 1 kHz,		0.2		%
X_{TALK}	Crosstalk	FFX stereo mode, <5 kHz, one channel driven at 1 W and other channel measured		80		dB
η	Peak efficiency, FFX mode	Po = 2 x 20 W into 8 Ω		90		%

2.3.2. Operating Specifications

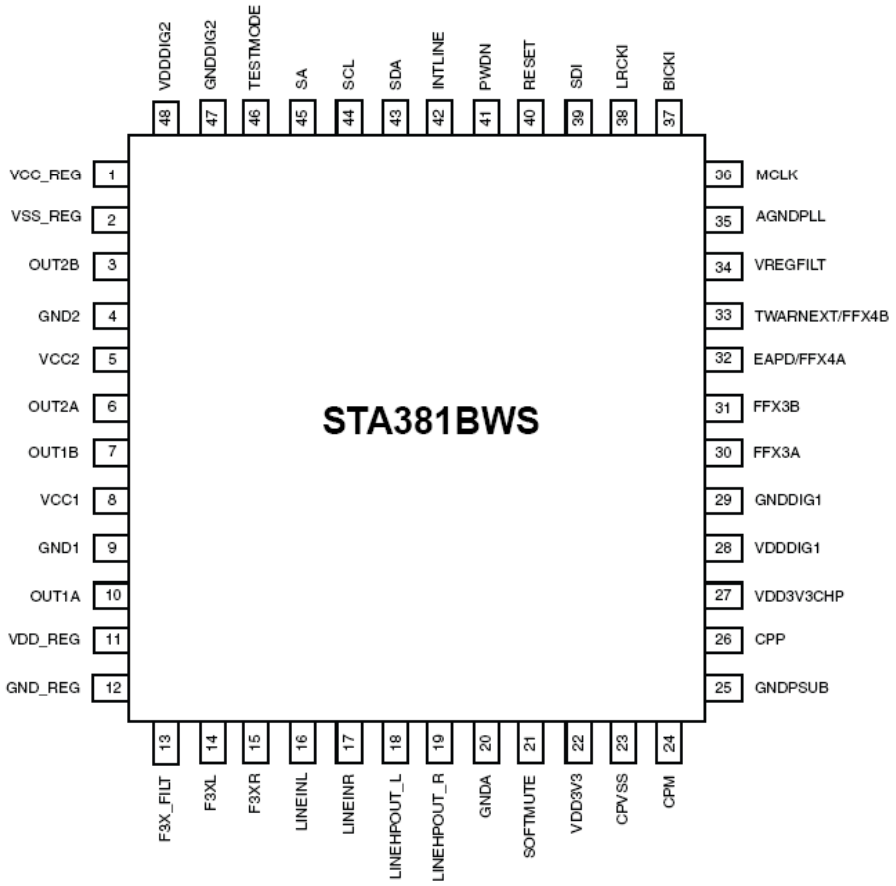
The specifications given in this section are valid for the operating conditions:

f = 1 kHz, T_{amb} = 25 °C, VDD3V3 = 3.3 V, R_{Line}= 5 kΩ, R_{Hp} = 32 Ω, unless otherwise specified.

Table 8. Electrical specifications for the analog section

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Vout	Output voltage for line out	G_v = 2.5, THD < 1%, Rload = 5 kΩ	1.9		2.1	Vrms
Pout	Output voltage for HP out	THD+N = 10%, G_v = 2.5, Rload = 32 Ω		40		mW
DR	Dynamic range for line out	Vout = 2 V_{RMS}, F_{in} = 200 Hz, V_{in} = 0.8 mV (-60 dBFs)		100		dB
X-Talk	Channel separation for line out	V_{out} = 2 Vrms, G_v = 2.5		75		dB
PSRR	Power supply rejection ratio	HP mode, P_0 = 15 mW		70		dB
		Line out mode, V_{Out} = 2 Vrms		70		
R_{in}	Line input resistance				30(1)	kΩ
THD+N	Total harmonic distortion + noise	HP mode, V_{out} = 200 mV_{RMS}, G_v = 2.5		0.03		%
		Line out mode, V_{Out} = 0.2 Vrms, G_v = 2.5		0.03		%

2.4. Pinning



VQFN 48 pin	TQFP 64 pin	Name	Type	Description
1	62	VCC_REG	POWER	VCC reg
2	64	VSS_REG	POWER	Vss reg, VCC_REG-3.3V
3	1- 2	OUT2B	OUTPUT	Half-bridge 2B output
4	3-4	GND2	POWER	Half-bridge 2A and 2B ground
5	5-6	VCC2	POWER	Half-bridge 2A and 2B supply
6	7-8	OUT2A	OUTPUT	Half-bridge 2A output
7	9-10	OUT1B	OUTPUT	Half-bridge 1B output
8	11-12	VCC1	POWER	Half-bridge 1A and 1B supply
9	13-14	GND1	POWER	Half-bridge 1A and 1B ground
10	15-16	OUT1A	OUTPUT	Half-bridge 1A output
11	17	VDD_REG	POWER	VDD reg 3.3 V
12	18	GND_REG	POWER	DC reg ground
13	21	F3X_FILT	POWER	F3X reference voltage
14	22	F3XL	OUTPUT	F3X analog out left channel
15	23	F3XR	OUTPUT	F3X analog out right channel
16	24	LINEINL	INPUT	Line in left channel
17	25	LINEINR	INPUT	Line in right channel
18	26	LINEHPOUT_L	OUTPUT	Headphone/line driver left channel
19	27	LINEHPOUT_R	OUTPUT	Headphone/line driver right channel
20	28	GNDA	POWER	Headphone/line driver power ground
21	29	SOFTMUTE	INPUT	Soft mute
22	30	VDD3V3	POWER	+3 V LDO power supply
23	31	CPVSS	POWER	-3.3 V charge pump pin
24	32	CPM	FILTER	CHP Cfly negative
25	35	GNDPSUB	POWER	Charge pump ground
26	36	CPP	FILTER	CHP Cfly positive
27	37	VDD3V3CHP	POWER	Charge pump power supply
28	38	VDDDIG1	POWER	I/O Ring power supply
29	39	GNDDIG1	POWER	Digital core ground

VQFN 48 pin	TQFP 64 pin	Name	Type	Description
30	40	FFX3A	OUTPUT	Digital PWM line out
31	41	FFX3B	OUTPUT	Digital PWM line out
32	42	FFX4A	OUTPUT	Digital PWM line out
33	43	FFX4B	OUTPUT	Digital PWM line out
34	44	VREGFILT	POWER	Digital VDD from core
35	45	AGNDPLL	POWER	PLL analog ground
36	46	MCLK	INPUT	PLL input clock
37	47	BICKI	INPUT	IIS serial clock
38	48	LRCKI	INPUT	IIS left/right clock
39	49	SDI	INPUT	IIS serial data input
40	50	RESET	INPUT	Reset
41	51	PWDN	INPUT	Device power-down 0 = power-down 1 = normal operation
42	52	INTLINE	OUTPUT	Fault interrupt
43	53	SDA	I/O	IIC serial data
44	54	SCL	INPUT	IIC serial clock
45	55	SA	INPUT	IIC select address (pull-down)
46	56	TEST_MODE	INPUT	This pin must be connected to ground (pull-down)
47	57	GNDDIG2	POWER	Digital I/O ground
48	58	VDDDIG2	POWER	Digital core LDO supply
	19, 20, 33, 34, 59, 60, 61	Not Connected	N.C.	

TS4962M (Optional 2,5W)

Features

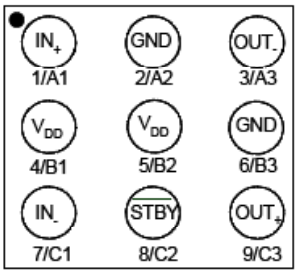
- Operating from V_{CC} = 2.4V to 5.5V
- Standby mode active low
- Output power: 3W into 4Ω and 1.75W into 8Ω with 10% THD+N max and 5V power supply.
- Output power: 2.3W @5V or 0.75W @ 3.0V into 4Ω with 1% THD+N max.
- Output power: 1.4W @5V or 0.45W @ 3.0V into 8Ω with 1% THD+N max.
- Adjustable gain via external resistors
- Low current consumption 2mA @ 3V
- Efficiency: 88% typ.
- Signal to noise ratio: 85dB typ.
- PSRR: 63dB typ. @217Hz with 6dB gain
- PWM base frequency: 250kHz
- Low pop & click noise
- Thermal shutdown protection
- Available in flip-chip 9 x 300µm (Pb-free)

Description

The TS4962M is a differential Class-D BTL power amplifier. It is able to drive up to 2.3W into a 4Ω load and 1.4W into a 8Ω load at 5V. It achieves outstanding efficiency (88%typ.) compared to classical Class-AB audio amps.

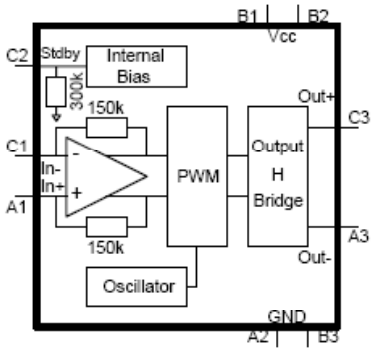
The gain of the device can be controlled via two external gain-setting resistors. Pop & click reduction circuitry provides low on/off switch noise while allowing the device to start within 5ms. A standby function (active low) allows the reduction of current consumption to 10nA typ.

Pin connections



IN+: positive differential input
IN-: negative differential input
VDD: analog power supply
GND: power supply ground
STBY: standby pin (active low)
OUT+: positive differential output
OUT-: negative differential output

Block diagram



3. POWER STAGE

The DC voltages required at various parts of the chassis and panel are provided by a main power supply unit. MB81 chassis can operate with PW05, IPS60, IPS70, IPS16, IPS17, IPS19, PW25, PW26, PW82-3, PW03, PW04, PW06, PW07 as main power supply and also with 12V adaptor.

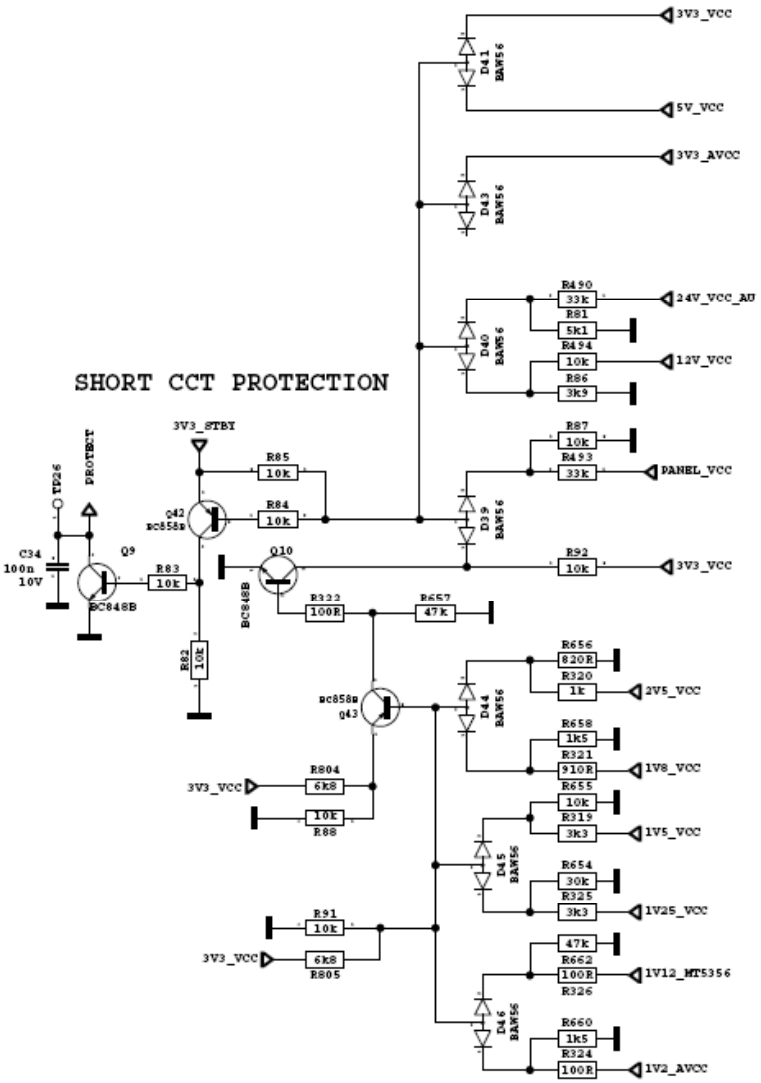
Which power board can be used for board to board or cable connection?

Board to board (BTB) : PW05, IPS60, IPS70, IPS16, IPS17, IPS19
Power Cable : PW25, PW26, PW82-3, PW03, PW04, PW06, PW07

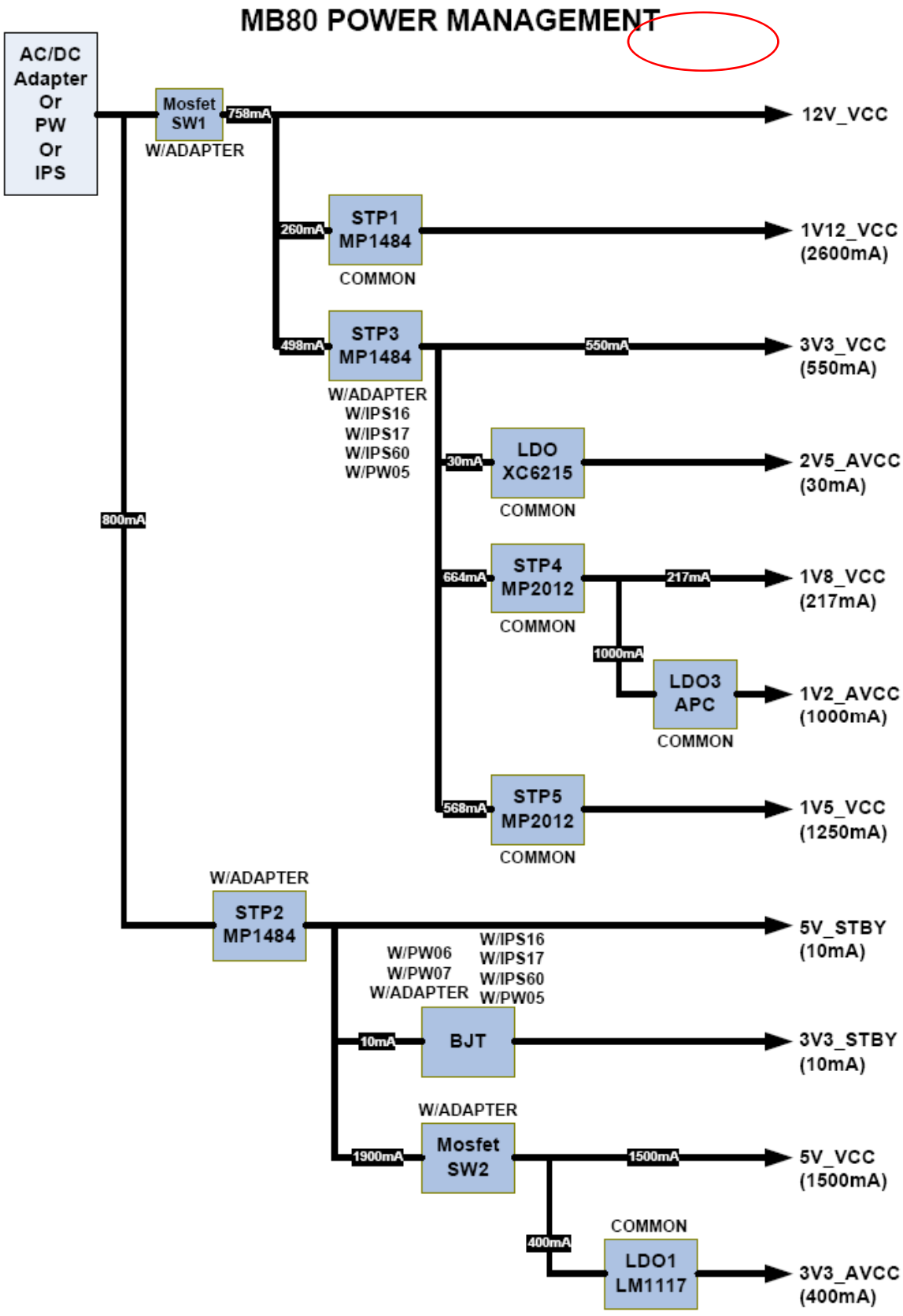
The power supplies generate 24V, 12V, 5V, 3,3V and 12V, 5V,3.3V stand by mode DC voltages. Power stage which is on-chassis generates 5V, 3V3 stand by voltage and 12V, 8V, 5V, 3V3, 2.5V, 1,8V and 1,2V supplies for other different parts of the chassis. Chassis block diagram is indicated below.

The blocks on power block diagram is using dependent to main supply. For PW26 and PW27 just common blocks are enough for proper operation.

Short CCT Protection Circuit
Short circuit protection is necessary for protecting chassis and main IC against damages when any Vcc supply shorts to ground. Protect pin should be logic high while normal operation. When there is a short circuit protect pin shold be logic low. After any short detection, SW forces LEDs on LED card to blink.


SHORT CCT PROTECTION
3V3_VCC
5V_VCC
3V3_AVCC
24V_VCC_AU
12V_VCC
PANEL_VCC
3V3_VCC
2V5_VCC
1V8_VCC
1V5_VCC
1V25_VCC
1V12_MT5356
1V2_AVCC
3V3_STBY
PROTECT
TP26
C34
100n
10V
Q9
BC848B
R83
10k
R82
10K
Q42
BC858B
R85
10k
R84
10k
Q10
BC848B
R333
100R
R657
47k
Q43
BC858B
R804
6k8
R88
10k
R91
10k
R805
6k8
D41
BAM56
D43
BAM56
D40
BAM56
D39
BAM56
D44
BAM56
D45
BAM56
D46
BAM56
R490
33k
R81
5k1
R494
10k
R86
3k9
R87
10k
R493
33k
R92
10k
R656
820R
R320
1k
R658
1k5
R321
910R
R655
10k
R319
3k3
R654
30k
R325
3k3
47k
R662
100R
R326
R660
1k5
R324
100R

3.1. Power Management



4. MICROCONTROLLER – MediaTek

4.1. Description

MT5365 (Main IC) (U1)

This document is mainly for audio quality (AQ) tuning and customization. We will introduce each AQ module enclosed in the red box of the following audio block diagram one by one in chapter 3. We will also include each module‟s control CLI and tuning tool with corresponding firmware and Flash AQ customization methods.

Before we go through each module introduction, we will briefly introduce the tuning and customization tools in the chapter 2.

Followed by chapter 3, we will include a Full-Watt manipulation example in chapter 4 that you can start your first AQ tuning exercise.

The MediaTek MT5356 family is a backend decoder and a TV controller and offers high integration for advanced applications. It combines a transport de-multiplexer, a high definition video decoder, an AC3 audio decoder, a dual-link LVDS/mini-LVDS transmitter, and an NTSC/PAL/SECAM TV decoder with a 3D comb filter (NTSC/PAL). The MT5356 enables consumer electronics manufactures to build high quality, low cost and feature-rich DTV.

World-Leading Audio/Video Technology: The MT5356 supports Full-HD MPEG1/2/4/DiviX/VC1/RM/H.264/AVS video decoder standards, and JPEG. The MT5356 also supports MediaTek MDDi™ de-interlace solution can reach very smooth picture quality for motions. A 3D comb filter added to the TV decoder recovers great details for still pictures. The special color processing technology provides natural, deep colors and true studio quality video. Also, the MT5356 family has built-in high resolution and high-quality audio codec.

Rich Features for High Value Products: The MT5356 family enables true single-chip experience. It integrates high-quality HDMI1.3 (partial HDMI1.4), high speed VGA ADC, dual-channel LVDS, USB2.0 receiver, Ethernet, TCON and panel overdrive.

Key Features:

1. Worldwide multi-standard analog TV demodulator
2. A transport demultiplexer
3. A muti-standard video decoder
4. An AC3/MPEG2 audio decoder
5. HDMI1.3 receiver (cover HDMI1.4 partial Spec)

HDMI 1.4 Spec.	Ethernet Channel	3D over HDMI	4Kx2K	Audio Return Channel	Additional Color Space
	Optional	Yes	No	Yes	Yes

6. Audio codec
7. TCON
8. Ethernet
9. Panel overdrive control
10. Local dimming

- Host CPU
  - ARM1176JZS-756MHz
  - 16K I-Cache and 16K D-Cache
  - 14K Boot ROM
  - JTAG ICE interface
  - Watch Dog timers

- Transport Demultiplexer
  - New generation 2 demux design
  - Supports two serial transport stream input with one serial transport stream output, or one parallel transport stream input
  - Supports ATSC, DVB-T, DVB-C transport stream input
  - Support DES / 3-DES / DVB / AES / Multi-2 de-scramblers
  - Up to 8 even/odd keys for descrambling
  - Supports 32 PID filters and 32 section filters
  - Supports 32 PID filters for recording
  - Supports hardware CRC-32 check
  - Supports PCR recovery function
  - Supports a micro-processor for stream process and video start code detection

- MPEG2 Decoder
  - MPEG MP@ML, MP@HL
  - Supports de-blocking filter

- MPEG1 Decoder

MPEG4 Decoder
  - ASP@L5

H.264 (MPEG4.10) HD Decoder (AVC)
  - MP@L4.0, HP@L4.0, constrained BP@L3 video standard

VC-1 (SMPTE421M)
  - MP@HL, AP@L3(Partial Support, support up to 1920x1080)

- WMV9 decoder MP@HL

DivX (XviD) Decoder

- DIVX3 / DIVX4 / DIVX5 / DIVX6 / DIVX HD

- AVS Decoder
  - Jizhun profile @Level 6.0.1
- RMVB Decoder
  - RealVideo8/9/10
- Soreson H.263
- Still Image decoding
  - JPEG (base-line or progressive)
- De-mosquito engine
  - 2D/3D for all AV inputs
- 2D Graphics
  - Supports multiple color modes
  - Point, horizontal/vertical line primitive drawings
  - Rectangle fill and gradient fill functions
  - Bitblt with transparent options
  - Alpha blending and optional pre-multiplied alpha composition Bitblt
  - Stretch Bitblt
  - YCbCr to RGB color space conversion
  - Support index to direct mode bitblt
- Image Resizer
  - Supports 16bpp/32bpp direct color format.
  - Supports 420/422 video format.
  - Supports 420/422/444 JPEG format.
  - Arbitrary ratio vertical/horizontal scaling of video, from 1/128X to 128X
  - Simple DMA.
- OSD Plane

- Three linking list OSDs with multiple color mode and two of them has up-scaler

- Video Plane
  - Supports video freeze and over scan.
  - Flesh tone management
  - Gamma correction
  - Color Transient Improvement (CTI)
  - 2D Peaking
  - Saturation/hue adjustment
  - Brightness and contrast adjustment
  - Black and White level extender
  - Adaptive Luma management
  - Automatic detect video, film and mixed-mode source
  - 3:2/2:2 pull down source detection
  - Supports FHD motion-adaptive de-interlace in 32bit dram interface
  - Supports excellent low angle image processing
  - Brilliant boundary shaping for moving object
  - Advanced non-linear panorama scaling.
  - Programmable zoom viewer
  - Progressive scan output
  - Supports alpha blending for OSD on video plane.
  - Dithering processing for flat panel display
  - Frame rate conversion.
  - Supports FHD panel and VGA dot-to-dot
  - Supports PIP/POP, (dual de-interlace, one HD and one SD)
- OD
  - Support 60Hz Full-HD and WXGA panel over drive.
- TCON
  - Flexible timing control with programmable timing
    i. Horizontal timing control
    ii. Vertical timing control
    iii. Multi-line timing control
    iv. Multi-frame timing control
  - Support gate power modulation timing
  - Support 1/2/4/8 frame inversion, 1-line inversion, 2-line inversion, and could up to 255-line dot inversion
- Local Dimming

- Block division: up to 800 total blocks, up to 100 horizontal blocks
- Support 50K ~ 50M SPI clock rate

■ LVDS

- Support 6/8/10/12-bit one-link, or 6/8/10-bit dual-link LVDS transmitter,
- Built-in spread spectrum for EMI performance
- Programmable panel timing output

■ Mini-LVDS

- Single port 6/8-bit 6 pairs mini-LVDS output for WXGA 60Hz panel
- Single port 6/8-bit 3 pairs mini-LVDS output for WXGA 60Hz panel
- Dual port 6/8-bit 3 pairs mini-LVDS output for WXGA 60Hz panel
- Single port 8bit 6 pairs mini-LVDS output for FHD 60Hz panel
- Dual port 8 bit 6 pair mini-LVDS output for FHD 60Hz panel
- Dual port 8bit 3 pairs mini-LVDS output for FHD 60Hz panel

■ CVBS In

- On-chip 54 MHz 10-bit video ADC
- Supports PAL (B,G,D,H,M,N,I,Nc), NTSC, NTSC-4.43, SECAM
- NTSC/PAL supports 3D/2D comb filter
- Built-in motion-adaptive 3D Noise Reduction
- VBI data slicer for CC/TT decoding
- Supports 2 S-Video.
- MT5366 support 3-channel CVBS. MT5365 support 2-channel CVBS.
- Supports SCART connector

■ VGA In

- Supports VGA input up to UXGA 162 MHz
- Supports full VESA standards

■ Component Video In

- Supports two component video inputs
- Supports 480i / 480p / 576i / 576p / 720p / 1080i / 1080p

■ Audio ADC

- MT5366 support 7-pair L/R input, MT5365 support 1-pair L/R input

■ Audio digital input

- MT5366 support 5 bit (10 channel) I2S audio input (muxed with GPIO), MT5365 support 2 bit (4 channel) I2S audio input (muxed with GPIO).

■ HDMI Receiver

- One channel HDMI1.4

v. Maximum data rate can be up to 3.3 GHz

vi. Support 3D video format

vii. Audio Return channel

- EIA/CEA-861B
- CEC

■ Video bypass

- TV bypass
- CVBS Monitor (any AV input)

■ TV audio demodulator

- Supports BTSC / EIA-J / A2 / NICAM / PAL FM / SECAM world-wide formats
- Standard automatic detection
- Stereo demodulation, SAP demodulation
- Mode selection (Main/SAP/Stereo)

■ Audio DAC

- MT5366 support 4-pair audio DACs, MT5365 support 2-pair audio DACs

■ DRAM Controller

- 16/32-bit DDR2/DDR3 interface, (MT5365 only support 16-bit DRAM)
- MT5365 Support DDR2 1026 MHz, DDR3 1188MHz. MT5366 Support DDR2 1026MHz, DDR3 1242MHz.
- Supports 512Mb or 1 Gb DDR2 DRAM device and 1Gb or 2Gb DDR3 device. MT5365 has 16-bit data bus offers up to 256MB space (one x16 DRAM device), and MT5366 has 32-bit data bus offers up to 512MB space (two x16 DRAM device).
- Supports DDR2-800/DDR2-1066/DDR3-1333/DDR3-1600 device

■ Audio DSP

- Supports Dolby Digital AC-3 decoding (ATSC)
- MPEG-1 layer I/II decoding
- Support WMA / HE-AAC
- Dolby Prologic II

- Audio output: 5.1ch + 2ch (down mix) + 2ch(bypass)
- Pink noise and white noise generator
- Equalizer
- Bass management
- 3D surround processing with virtual surround
- Audio and video lip synchronization
- Supports bass/treble
- Automatic volume control
- MT5366 supports 5-bit (10-channel) main audio I^2S output interface, MT5365 support 2-bit (4-channel) main audio I^2S output interface: each of these channels is up to 24-bit resolution.

■ S/PDIF interface

- Support SPDIF in bypass
- One SPDIF out

■ Analog TV IF Demodulator

- Supports world-wide analog TV standard
- Accept Low IF frequency
- Full digital AGC control and carrier recovery
- Embedded SAW filter and IF Amplifier. Cost effective TV front-end structure and no more costs on

viii. External analog SAW filters (Video/Audio)

ix. External analog IF demodulator

x. Extra peripheral circuit on CVBS signal data path

xi. External SAW filter and IF VGA on tuner

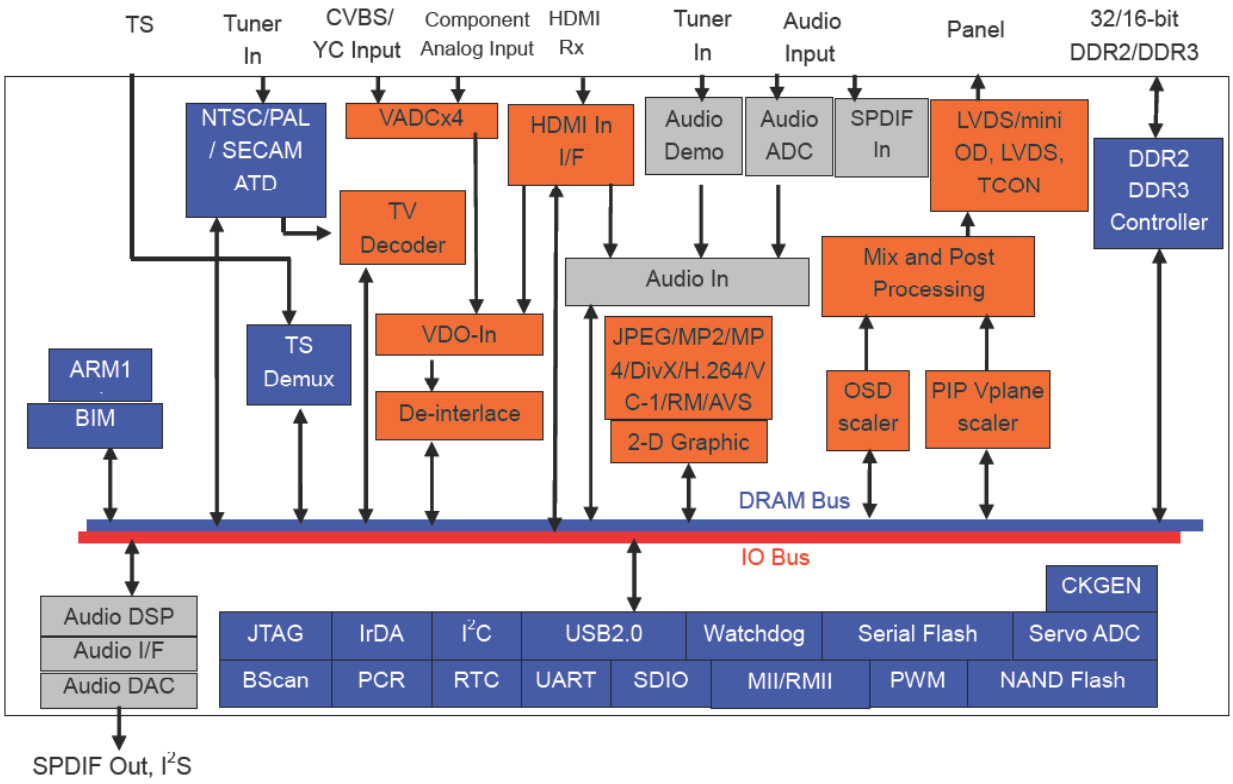
■ Peripherals

- MT5366 support three built-in UARTs with Tx and Rx FIFO, MT5365 support two UART (one is muxed with GPIO).
- MT5366 support MII/RMII interface (built-in Ethernet MAC), MT5365 support RMII only.
- Seven basic serial interfaces; one is for the tuner, one is the master for general purpose, and one is the slave for VGA DDC, the other four extra slave serial interfaces used for HDMI EDID data (three are muxed with GPIO).
- MT5366 support three PWMs, MT5365 support two PWMs (one is muxed with GPIO).
- IR receiver
- Real-time clock and watchdog controller
- Built-in 2-link USB2.0/1.1,USB port0 supports external hub,
- Built-in uP for standby mode
- Support SDIO interface pin muxed with smart card
- Supports two serial flash or one serial and one NAND flash
- MT5366 supports six-input low-speed ADC, MT5365 support five-input low-speed ADC.
- Supports boundary scan (JTAG)

■ IC Outline

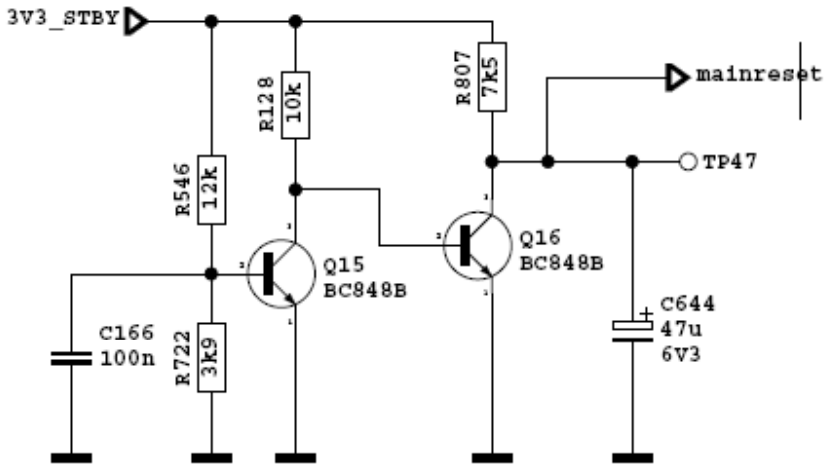
- The MT5366 is 21x21mm PBGA Package, MT5365 is 256-pin LQFP package with EPAD
- 3.3V/1.12V/1.2V and 1.8V for DDR2 or 1.5V for DDR3

4.2. MediaTek Block Diagram



4.3. Reset Circuit

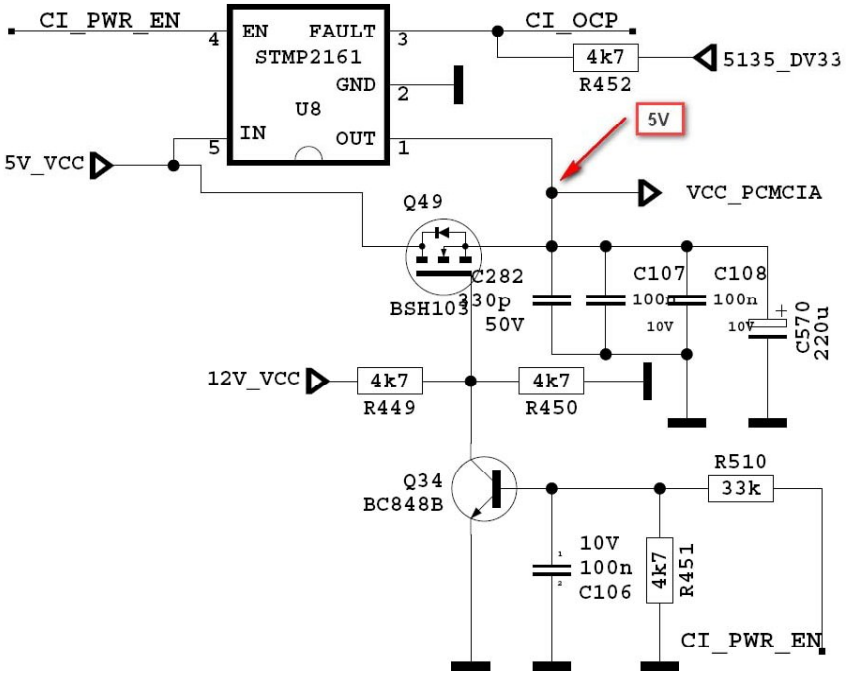
Reset circuit using for initiliazing main MediaTek IC. Reset condition is high and nomal working condition is low for RESET pin.



5. CI INTERFACE

CI Interface Power Switch:

It is used for CI module supply, when Module is inserted (it means CI detect is low) This circuit is opened or closed by CI_POWER_CTRL port of main uController

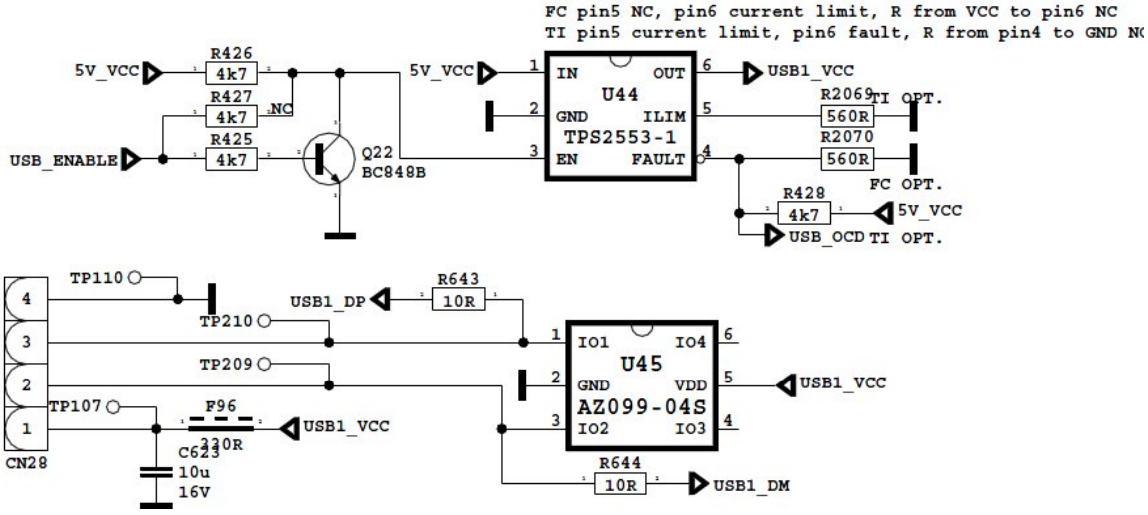


6. USB INTERFACE

Main Concept IC has integrated 1 USB 2.0 interface. It is used for USB connectivity for last user. Last user Also digital channels can be record to externall storage device by this interface. All SW files can be updated with interface.

USB circuit has 3 main parts

- Integrated USB 2.0 Host interface of D3K
- Protection IC
- Over Curent Protection IC



7. DDR3 SDRAM NTC-DDR3-1Gb-D-R12

Description:

The 1Gb Double-Data-Rate-3 (DDR3/L) B-die DRAMs is double data rate architecture to achieve high-speed operation. It is internally configured as an eight bank DRAM.

The 1Gb chip is organized as 16Mbit x 8 I/Os x 8 banks or 8Mbit x 16 I/Os x 8 bank devices. These synchronous devices achieve high speed double-data-rate transfer rates of up to 2133 Mb/sec/pin for general applications.

The chip is designed to comply with all key DDR3/L DRAM key features and all of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and ___falling). All I/Os are synchronized with a single ended DQS or differential DQS pair in a source synchronous fashion.

These devices operate with a single 1.5V ± 0.075V &1.35V -0.067/+0.1V power supply and are available in BGA packages.

Features:

- 1.35V -0.067/+0.1V &1.5V ± 0.075V (JEDEC Standard Power Supply)
- 8 Internal memory banks (BA0- BA2)
- Differential clock input (CK, $\overline{CK}$)
- Programmable $\overline{CAS}$ Latency: 5, 6, 7, 8, 9, 10, 11, 12, 13, (14)
- POSTED CAS ADDITIVE Programmable Additive Latency: 0, CL-1, CL-2
- Programmable Sequential / Interleave Burst Type
- Programmable Burst Length: 4, 8
- 8n-bit prefetch architecture
- Output Driver Impedance Control
- Differential bidirectional data strobe
- Write Leveling
- OCD Calibration
- Dynamic ODT (Rtt_Nom & Rtt_WR)
- Auto Self-Refresh
- Self-Refresh Temperature
- RoHS Compliance
- Lead-Free and Halogen-Free
- Packages:
  78-Ball BGA for x8 components
  96-Ball BGA for x16 components
- Operation Temperture
  Commerical grade (0℃ ≦TC≦95℃)
  - BE, CF, DH, EI, FK
  Industial grade (-40℃ ≦TC≦95℃)
  - CFI, DHI

Pinning 78 balls BGA Package (x8):

x 8

1	2	3		7	8	9
VSS	VDD	NC	A	NU/$\overline{TDQS}$	VSS	VDD
VSS	VSSQ	DQ0	B	DM/TDQS	VSSQ	VDDQ
VDDQ	DQ2	DQS	C	DQ1	DQ3	VSSQ
VSSQ	DQ6	$\overline{DQS}$	D	VDD	VSS	VSSQ
VREFDQ	VDDQ	DQ4	E	DQ7	DQ5	VDDQ
NC	VSS	$\overline{RAS}$	F	CK	VSS	NC
ODT	VDD	$\overline{CAS}$	G	$\overline{CK}$	VDD	CKE
NC	$\overline{CS}$	$\overline{WE}$	H	A10/AP	ZQ	NC
VSS	BA0	BA2	J	NC	VERFCA	VSS
VDD	A3	A0	K	A12/$\overline{BC}$	BA1	VDD
VSS	A 5	A2	L	A1	A4	VSS
VDD	A7	A9	M	A11	A6	VDD
VSS	$\overline{RESET}$	A13	N	NC	A8	VSS

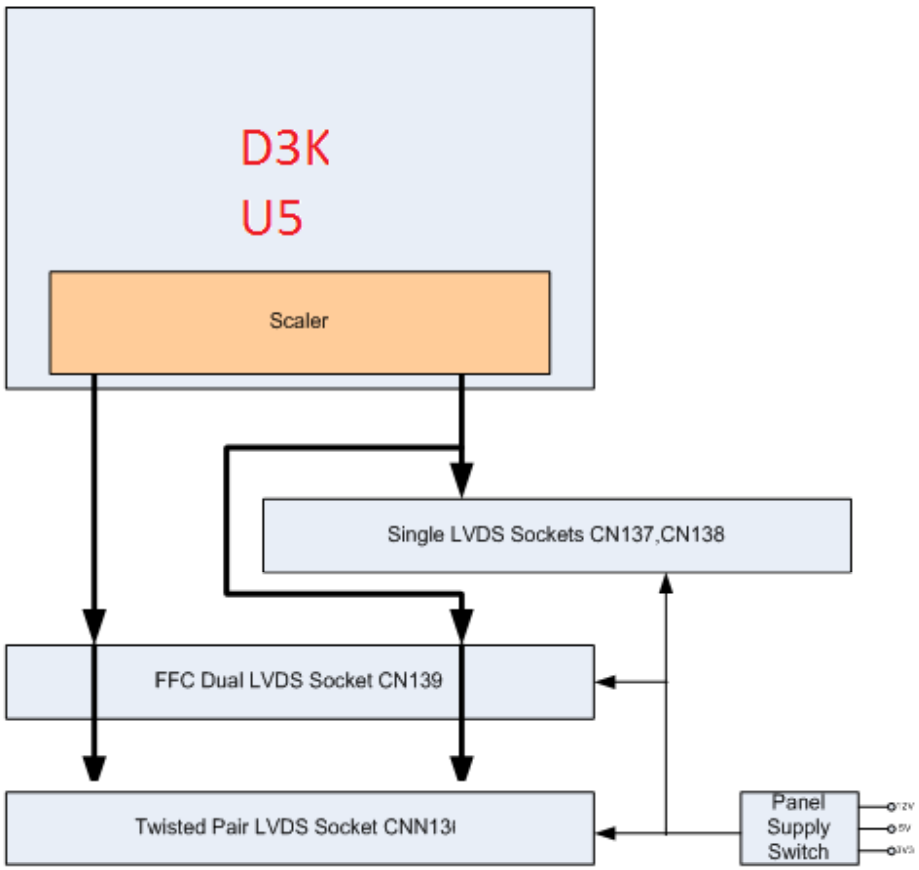
Pinning 78 balls BGA Package (x8):

x 16

1	2	3		7	8	9
VDDQ	DQU5	DQU7	A	DQU4	VDDQ	VSS
VSSQ	VDD	VSS	B	$\overline{DQSU}$	DQU6	VSSQ
VDDQ	DQU3	DQU1	C	DQSU	DQU2	VDDQ
VSSQ	VDDQ	DMU	D	DQU0	VSSQ	VDD
VSS	VSSQ	DQL0	E	DML	VSSQ	VDDQ
VDDQ	DQL2	DQSL	F	DQL1	DQL3	VSSQ
VSSQ	DQL6	$\overline{DQSL}$	G	VDD	VSS	VSSQ
VREFDQ	VDDQ	DQL4	H	DQL7	DQL5	VDDQ
NC	VSS	$\overline{RAS}$	J	CK	VSS	NC
ODT	VDD	$\overline{CAS}$	K	$\overline{CK}$	VDD	CKE
NC	$\overline{CS}$	$\overline{WE}$	L	A10/AP	ZQ	NC
VSS	BA0	BA2	M	NC	VREFCA	VSS
VDD	A3	A0	N	A12/$\overline{BC}$	BA1	VDD
VSS	A 5	A2	P	A1	A4	VSS
VDD	A7	A9	R	A11	A6	VDD
VSS	$\overline{RESET}$	NC	T	NC	A8	VSS

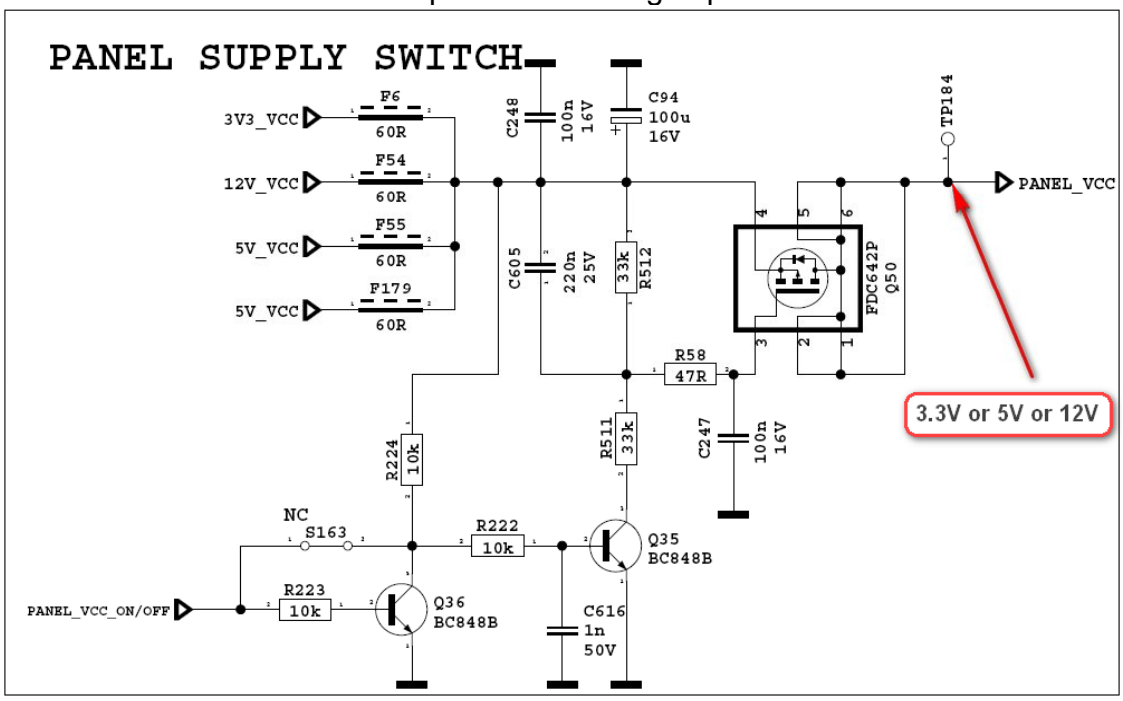
8. SCALER AND LVDS SOCKETS

8.1. LVDS sockets Block Diagram



8.2. Panel Supply Switch Circuit

This switch is used to open and close panel supply of TCON. It is controlled by port of main ucontroller. Also with this circit panel sequency could be adjusted correctly. 3 panel supplys are connected to this circuit. All of them are optional according to panels.



9. NAND FLASH MEMORY – K9F1G08U0D

9.1. General Description

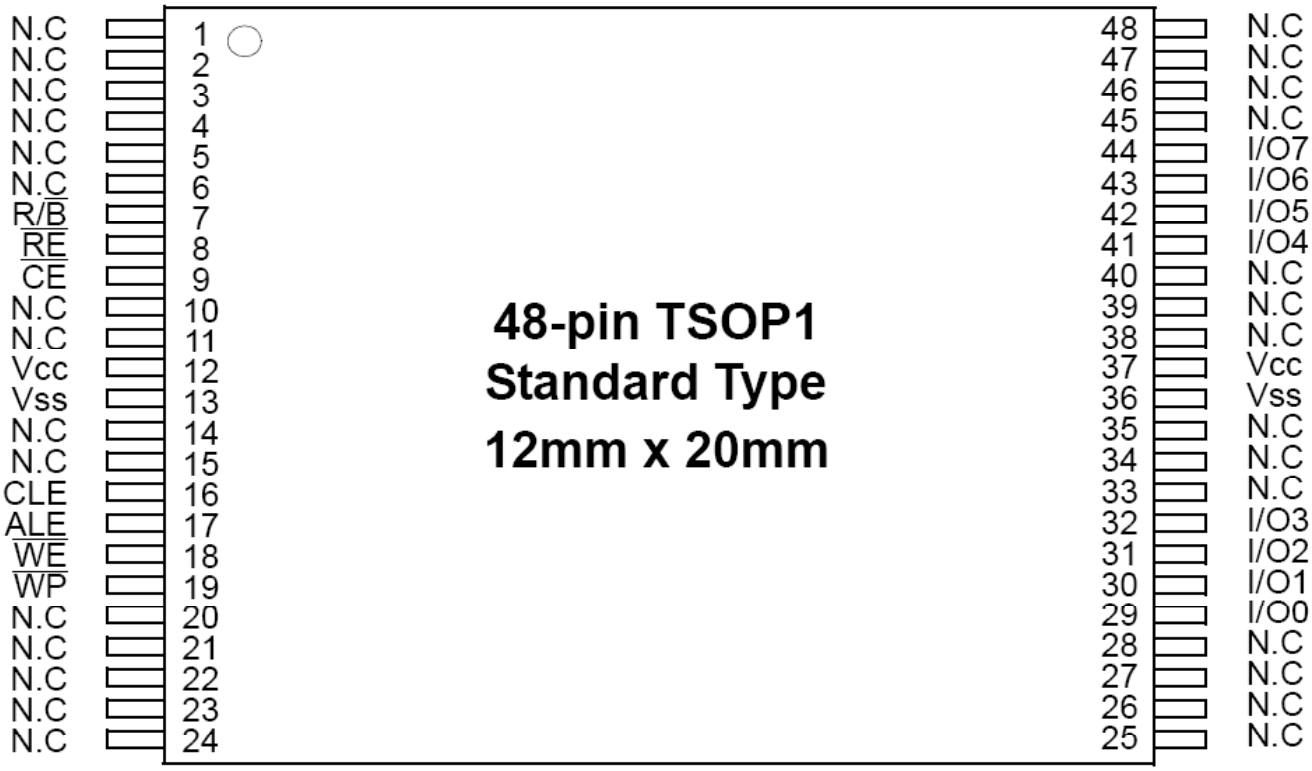
Offered in 128Mx8bit, the K9F1G08X0D is a 1G-bit NAND Flash Memory with spare 32M-bit. Its NAND cell provides the most costeffective solution for the solid state application market. A program operation can be performed in typical 250μs on the (2K+64)Byte page and an erase operation can be performed in typical 2ms on a (128K+4K)Byte block. Data in the data register can be read out at 30ns cycle time per Byte. The I/O pins serve as the ports for address and data input/output as well as command input. The onchip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. Even the write-intensive systems can take advantage of the K9F1G08X0D′s extended reliability by providing ECC(Error Correcting Code) with real time mapping-out algorithm. The K9F1G08X0D is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable app.lications requiring non-volatility.

9.2. Features

- Voltage Supply
  - 3.3V Device(K9F1G08U0D) : 2.7V ~ 3.6V
- Organization
  - Memory Cell Array : (128M + 4M) x 8bit
  - Data Register : (2K + 64) x 8bit
- Automatic Program and Erase
  - Page Program : (2K + 64)Byte
  - Block Erase : (128K + 4K)Byte
- Page Read Operation
  - Page Size : (2K + 64)Byte
  - Random Read :35µs(Max.)
  - Serial Access : 30ns(Min.)
- Fast Write Cycle Time
  - Page Program time : 250µs(Typ.)
  - Block Erase Time : 2ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  -Endurance & Data Retention : Refor to the gualification
  -ECC regnirement : 1 bit / 528bytes
- Command Driven Operation
- Unique ID for Copyright Protection
- Package :
  - K9F1G08U0D-SCB0/SIB0 : Pb-FREE PACKAGE
    48 - Pin TSOP I (12 x 20 / 0.5 mm pitch)
  - K9F1G08U0D-HCB0/HIB0 : Pb-FREE PACKAGE
    63 FBGA (9 x 11 / 0.8 mm pitch)

9.3. Pinning

K9F1G08X0D-SCB0/SIB0



10. I-LM1117/LM 800mA Low-Dropout Linear Regulator

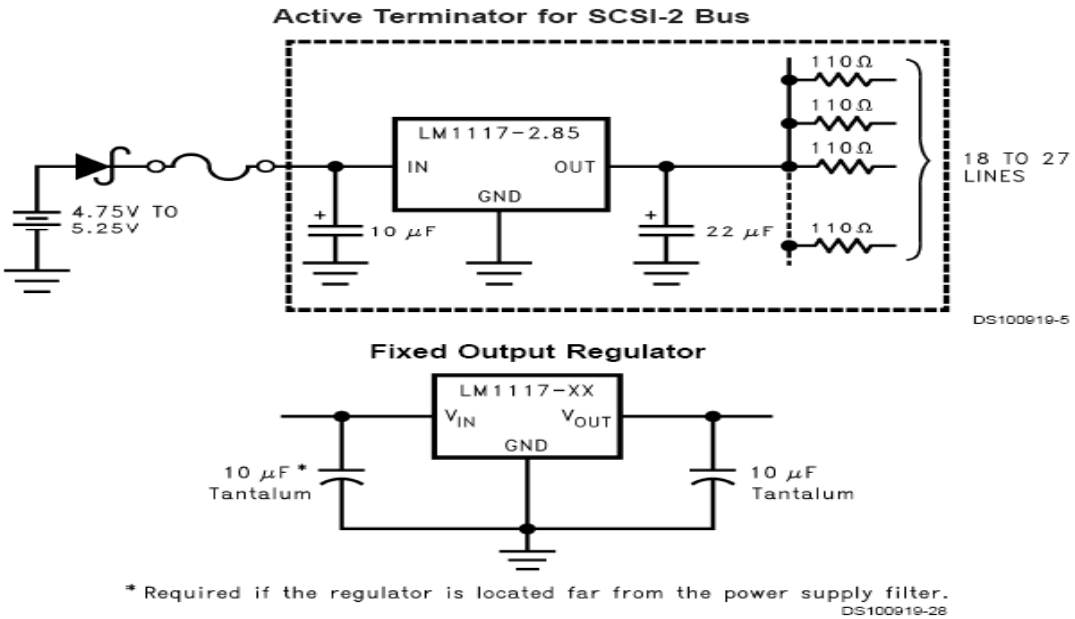
The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry standard LM317.
The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within ±1%. The LM1117 series is available in SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10μF tantalum capacitor is required at the output to improve the transient response and stability.

Features

Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
-- Space Saving SOT-223 Package
-- Current Limiting and Thermal Protection
-- Output Current 800mA
-- Line Regulation 0.2% (Max)
-- Load Regulation 0.4% (Max)
-- Temperature Range
— LM1117 0°C to 125°C
— LM1117I −40°C to 125°C

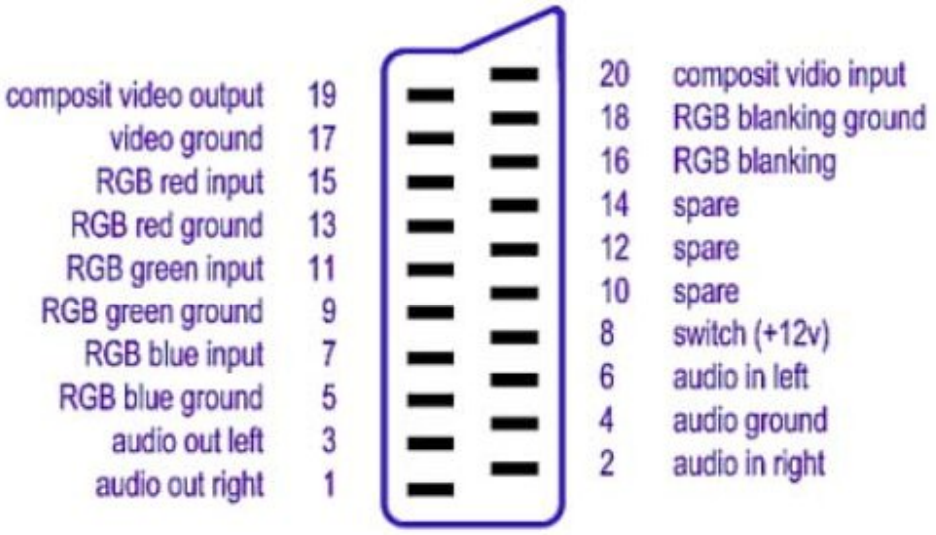
Applications

n 2.85V Model for SCSI-2 Active Termination
n Post Regulator for Switching DC/DC Converter
n High Efficiency Linear Regulators
n Battery Charger
n Battery Powered Instrumentation

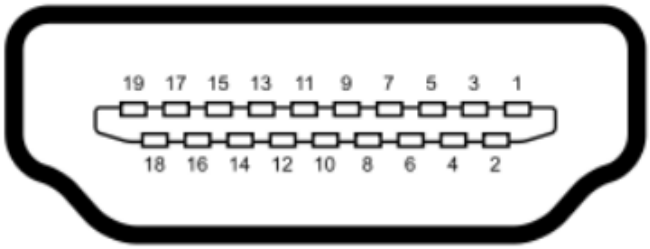


11. CONNECTORS

11.1. SCART (SC1)

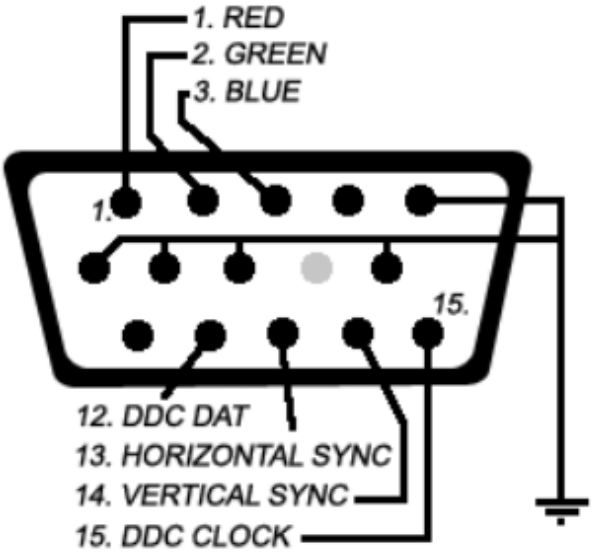


11.2. HDMI (CN707,CN708)



Pin Number	Signal Name	Pin Number	Signal Name
1	TMDS Data 2+	20	SHELL
2	TMDS Data 2 Shield	19	Hot Plug Detect
3	TMDS Data 2-	18	+5V Power
4	TMDS Data 1+	17	Ground
5	TMDS Data 1 Shield	16	DDC Data
6	TMDS Data 1-	15	DDC Clock
7	TMDS Data 0+	14	No Connect
8	TMDS Data 0 Shield	13	CEC
9	TMDS Data 0-	12	TMDS Clock-
10	TMDS Clock+	11	TMDS Clock Shield

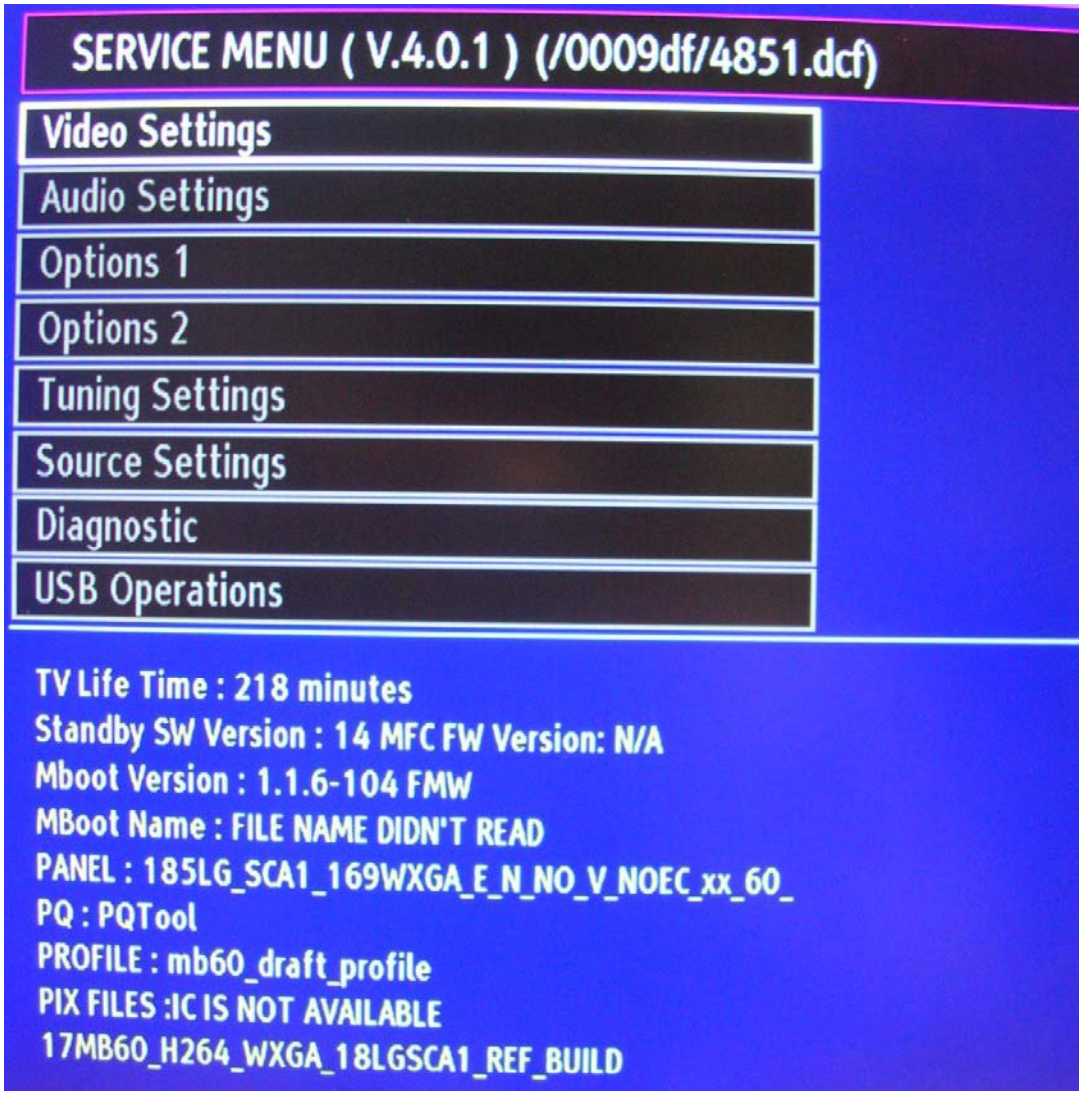
11.3. VGA (CN711)



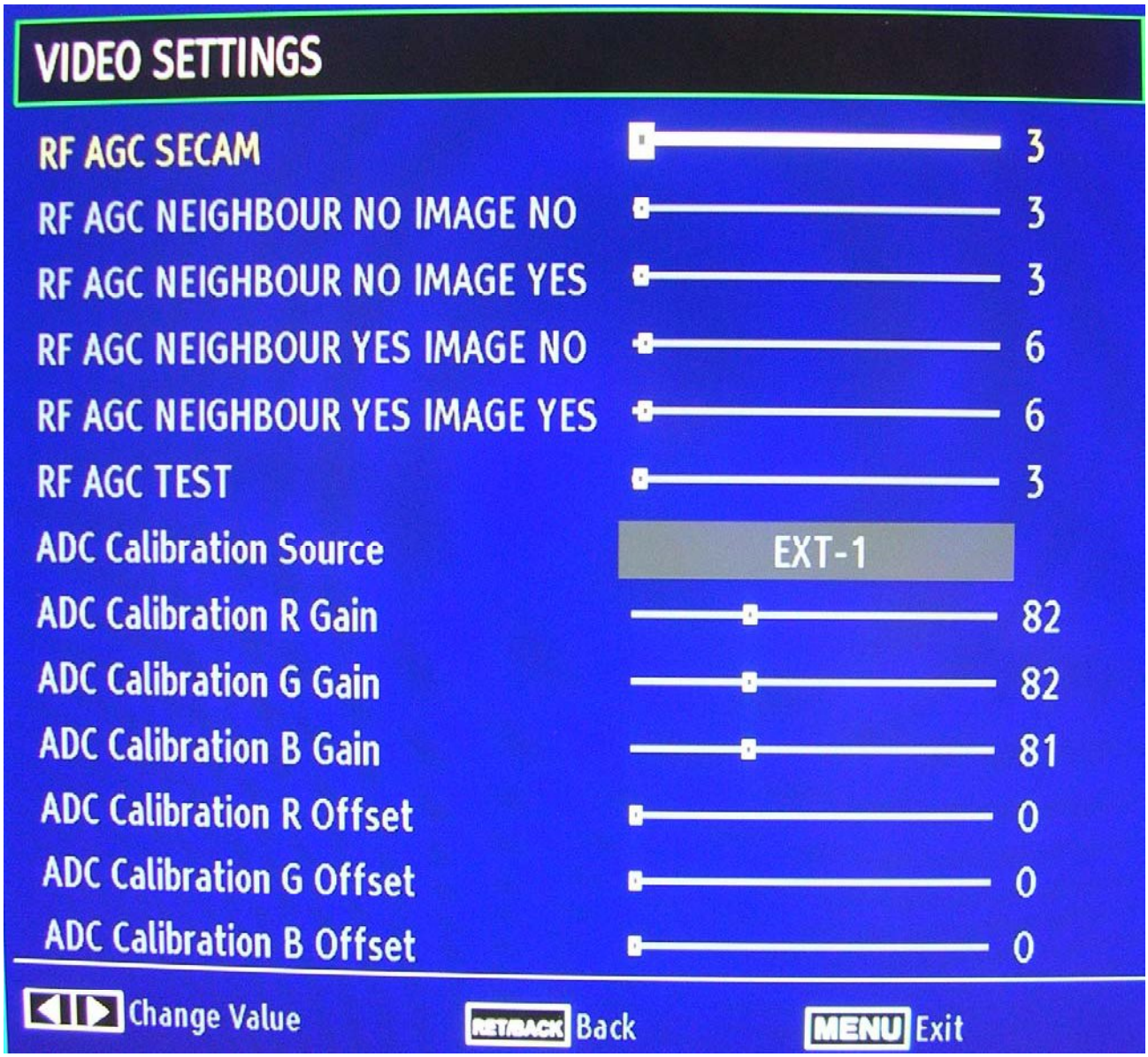
12. SERVICE MENU SETTINGS

In order to reach service menu, First Press **“MENU”** Then press the remote control code two times, which is **“4725”**.

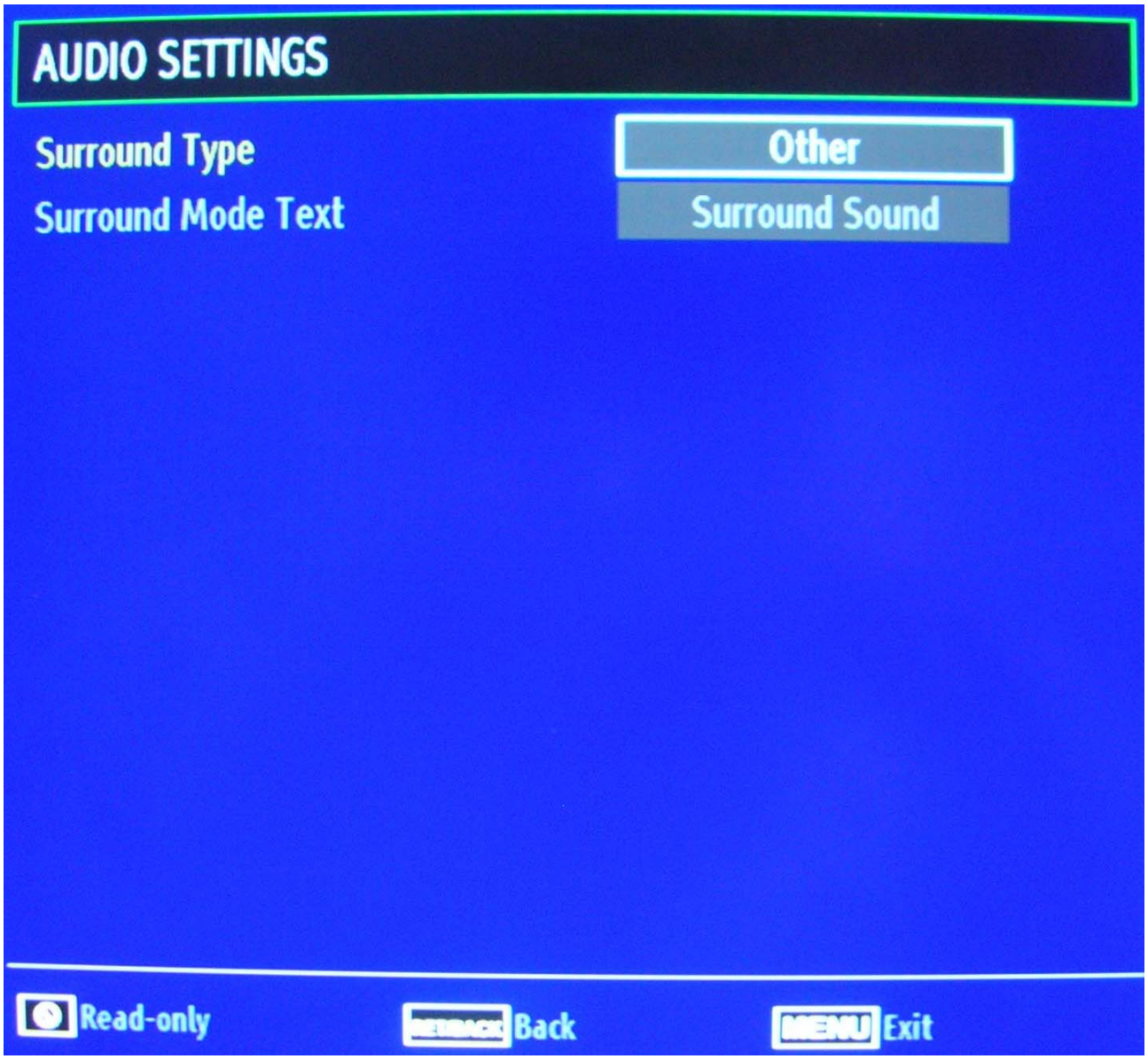
In first screen following items can be seen:



12.1. Video Settings

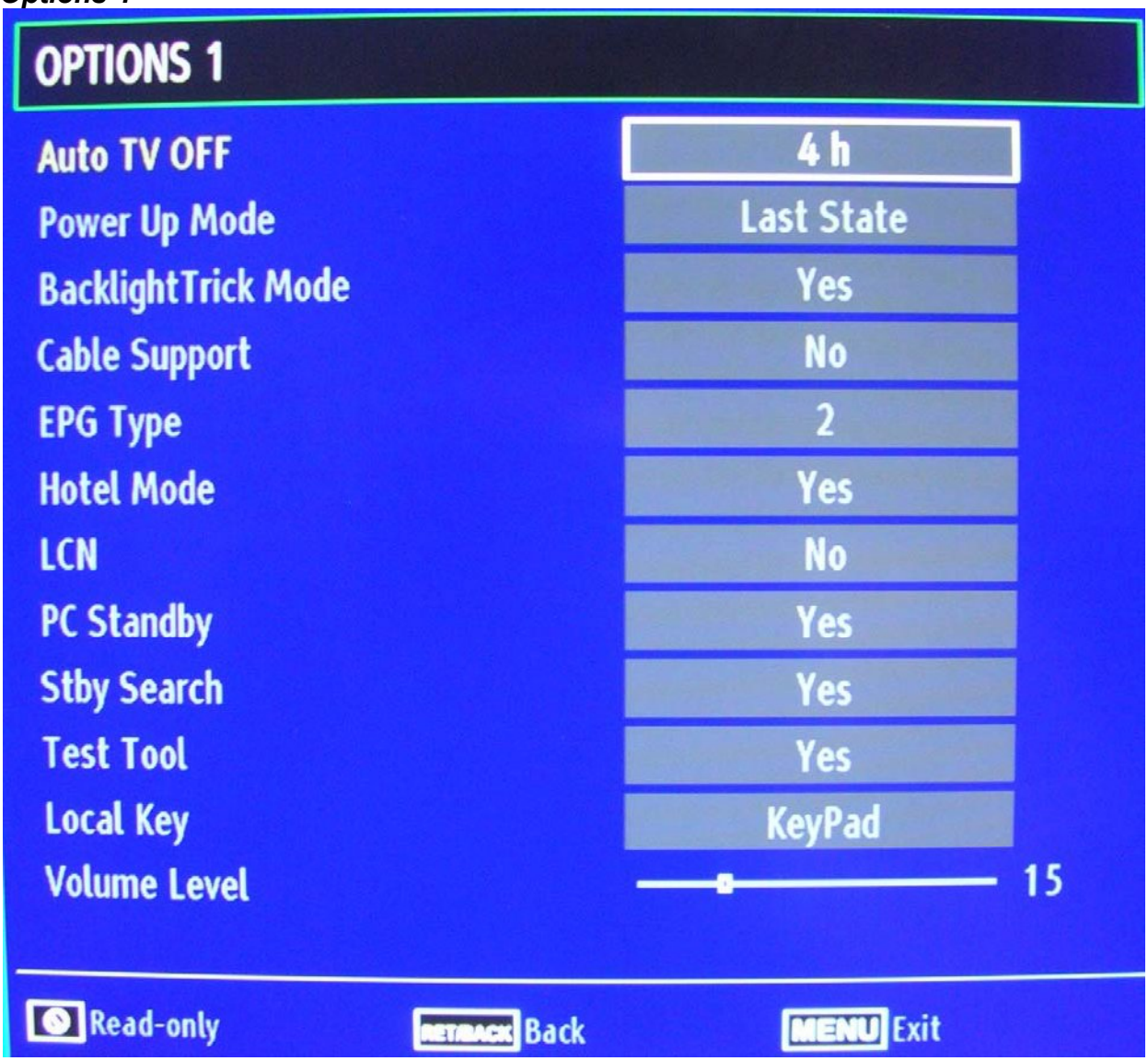


12.2. Audio Settings

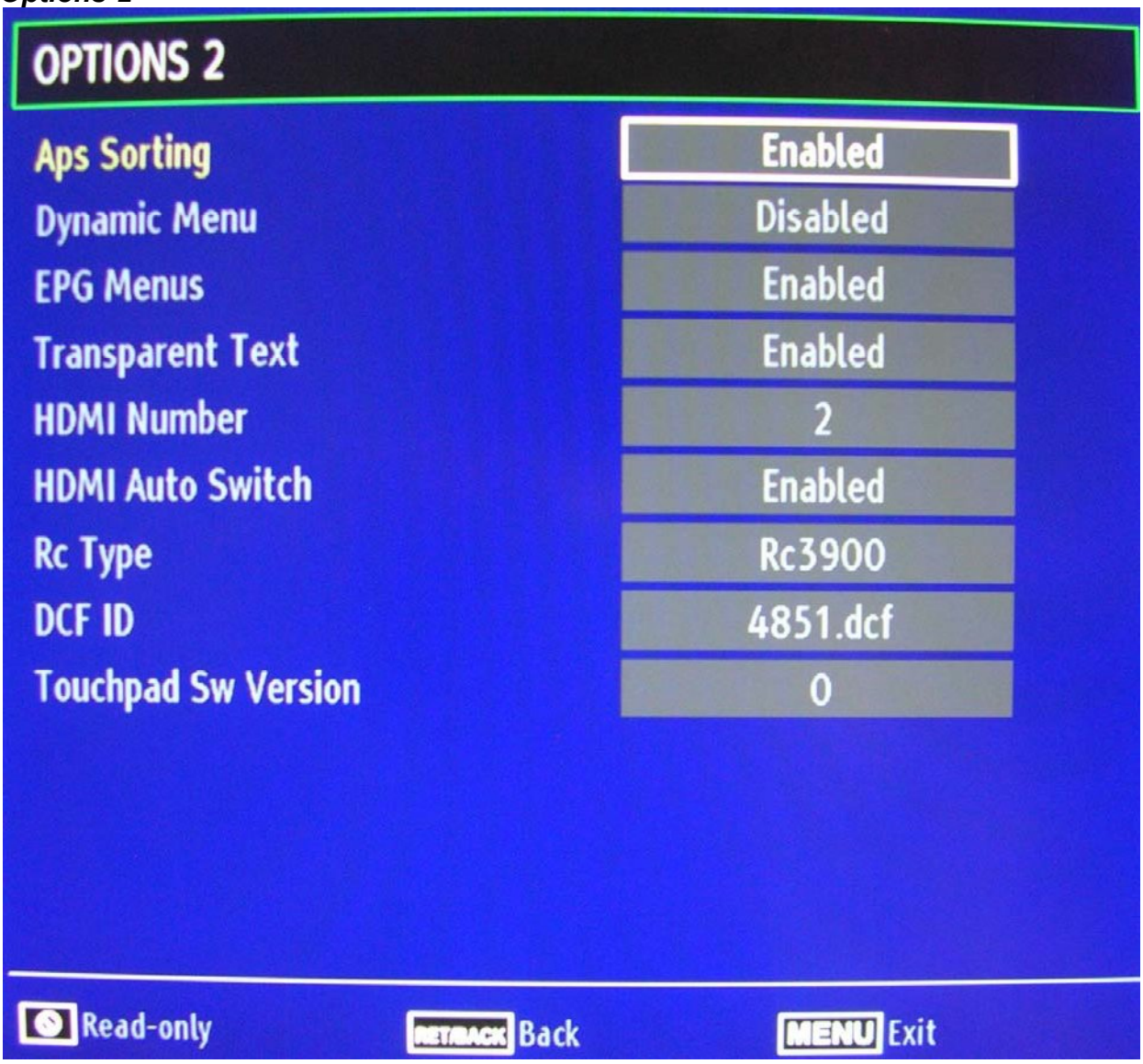


12.3. Options

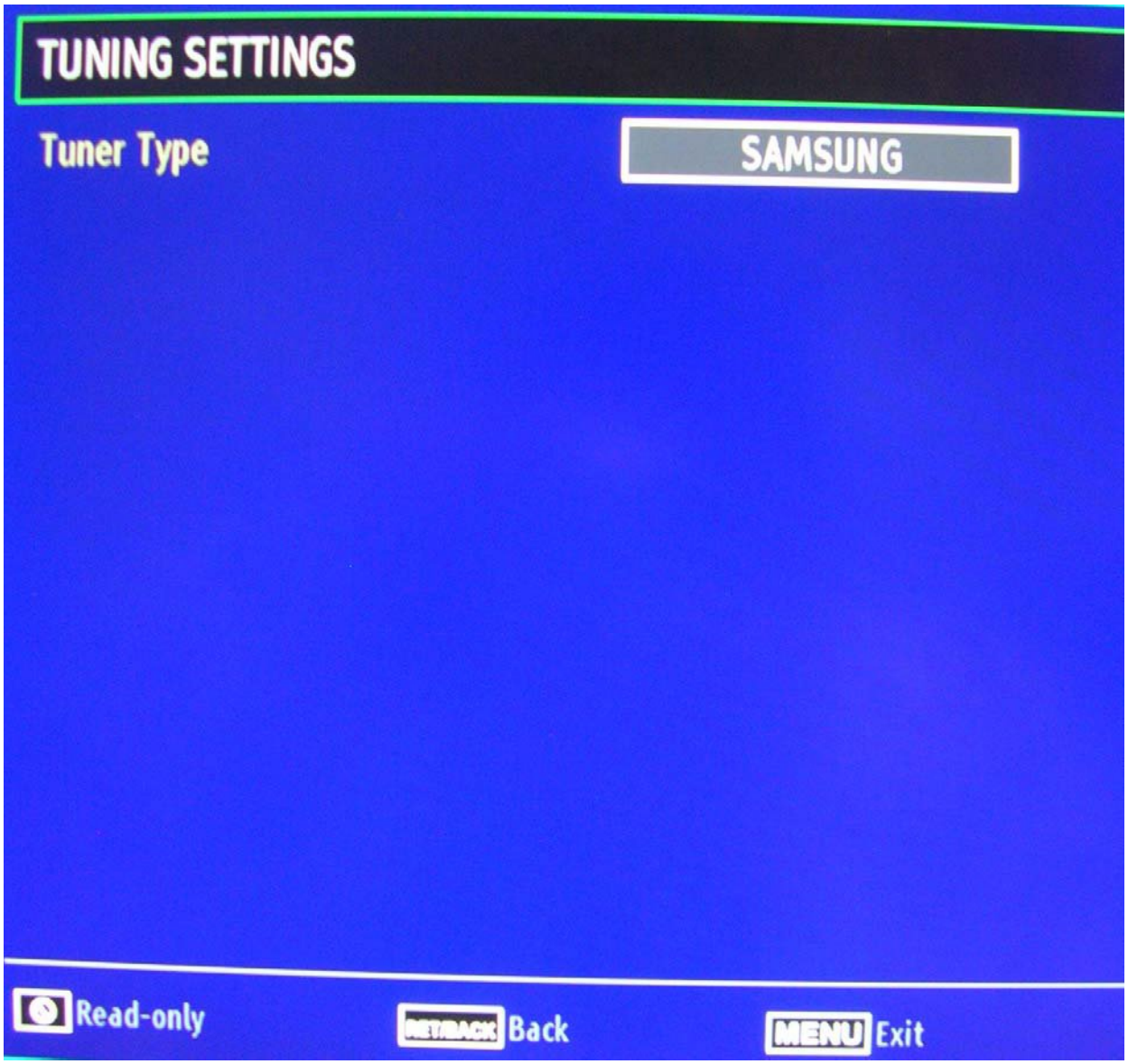
Options-1



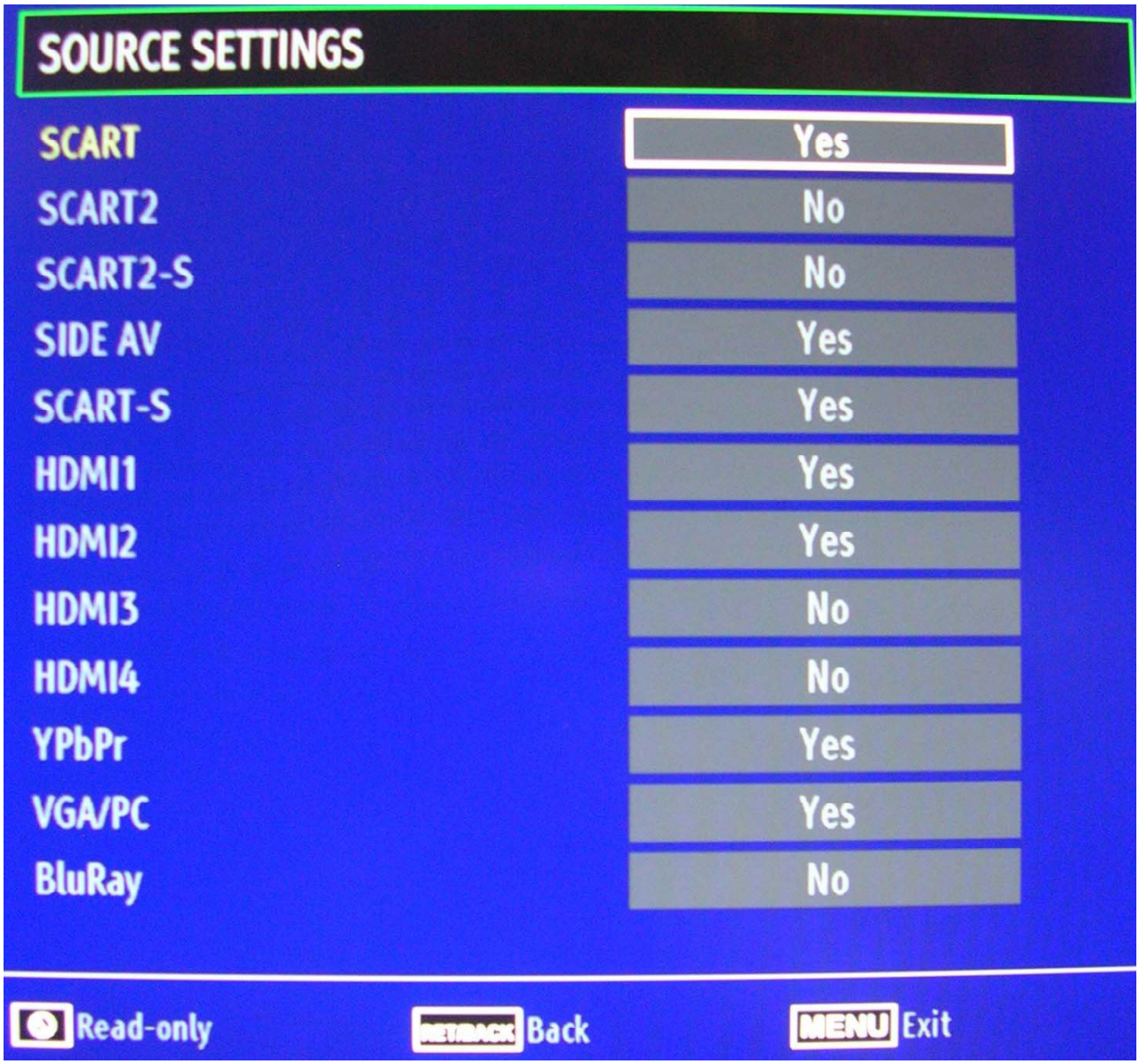
Options-2


OPTIONS 2
Aps Sorting
Enabled
Dynamic Menu
Disabled
EPG Menus
Enabled
Transparent Text
Enabled
HDMI Number
2
HDMI Auto Switch
Enabled
Rc Type
Rc3900
DCF ID
4851.dcf
Touchpad Sw Version
0
Read-only
RETURN/BACK Back
MENU Exit

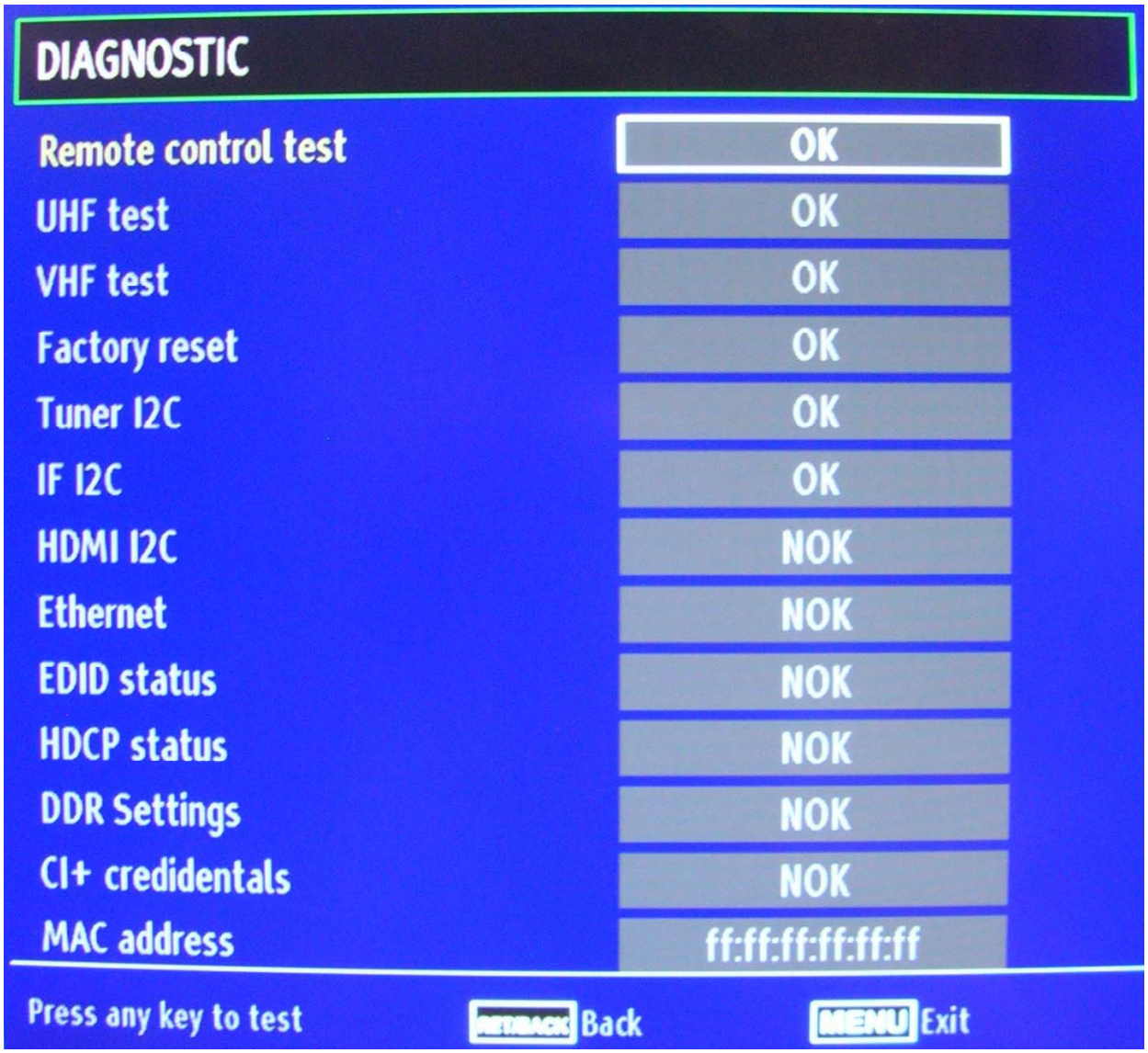
12.4. Tuning Settings



12.5. Source Settings



12.6. Diagnostic



12.7. USB Operations

USB operations option can not be used directly. It can be used for updating panel tool, hw congiguration etc.

13. SOFTWARE UPDATE

In MB81 project there is only one software. From following steps software update procedure can be seen:

1. MB81.bin directly inside of a flash memory(not in a folder).
2. Put flash memory to the tv when tv is powered off.
3. Power on the and pree OK button on the remote control when the tv is opened.
4. If First Time Installition screen comes, it means software update procedure is succesful.

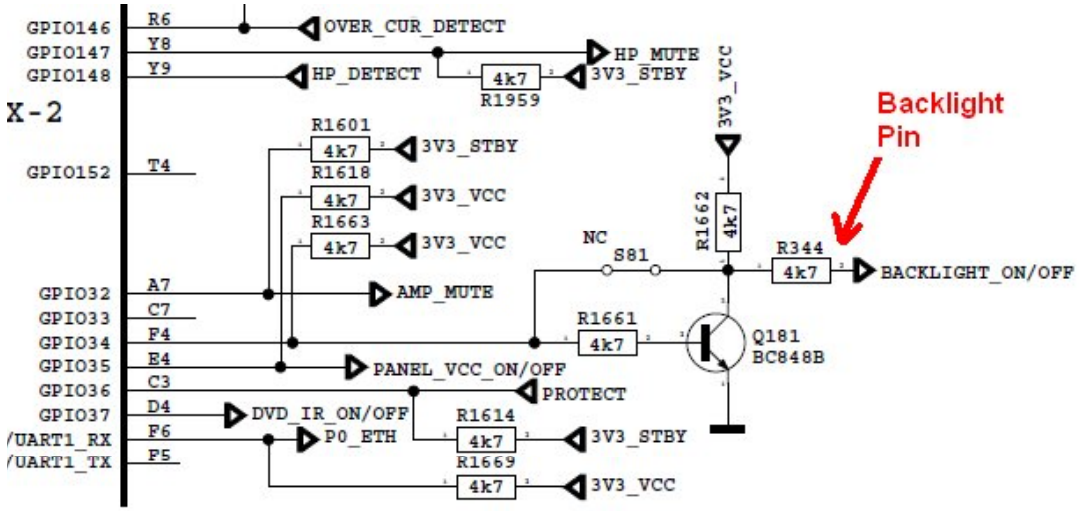
14. TROUBLESHOOTING

14.1. No Backlight Problem

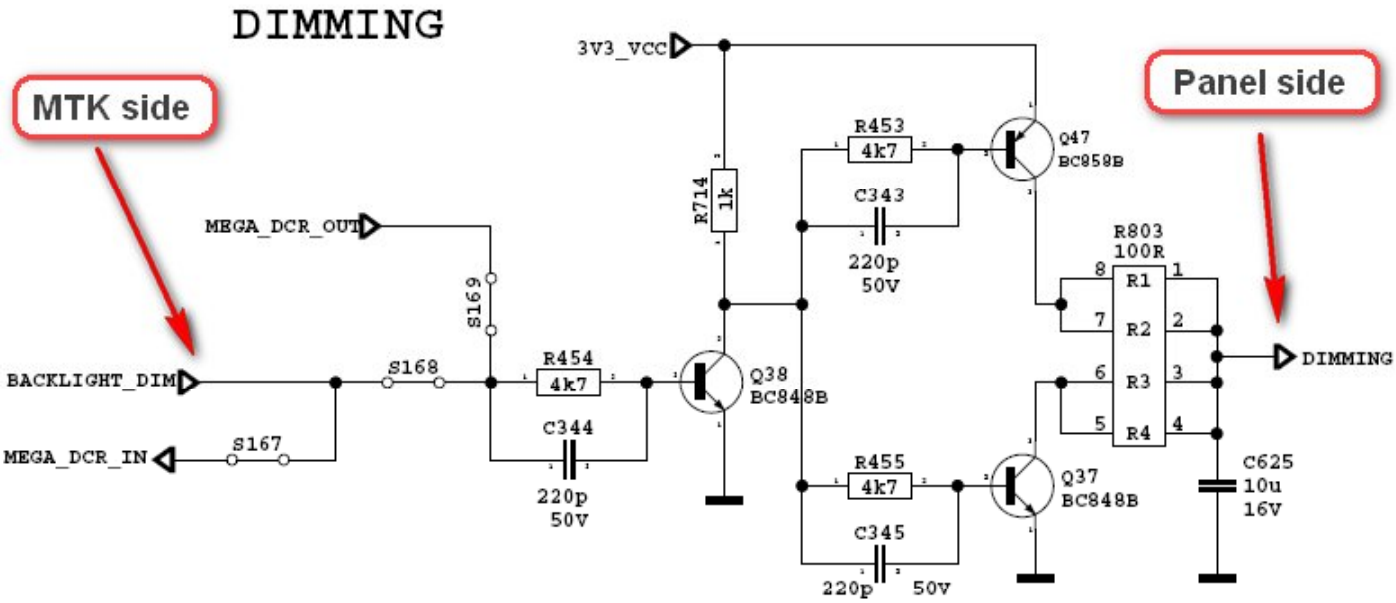
Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible couses: Backlight pin, dimming pin, backlight supply, stby on/off pin

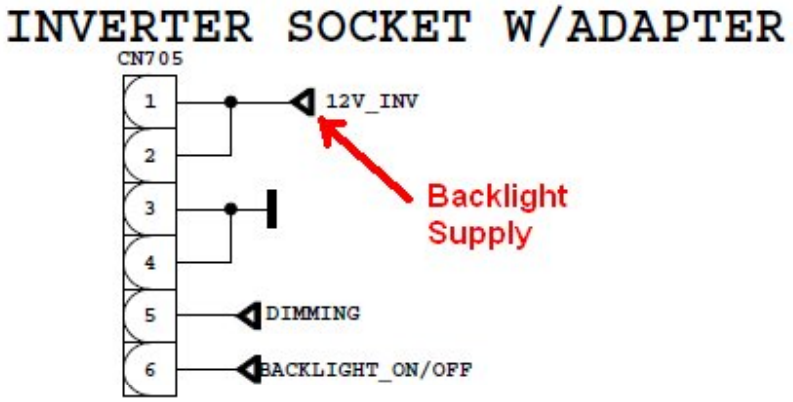
Backlight pin should be high in open position. If it is low, please check Q181 and panel cables.



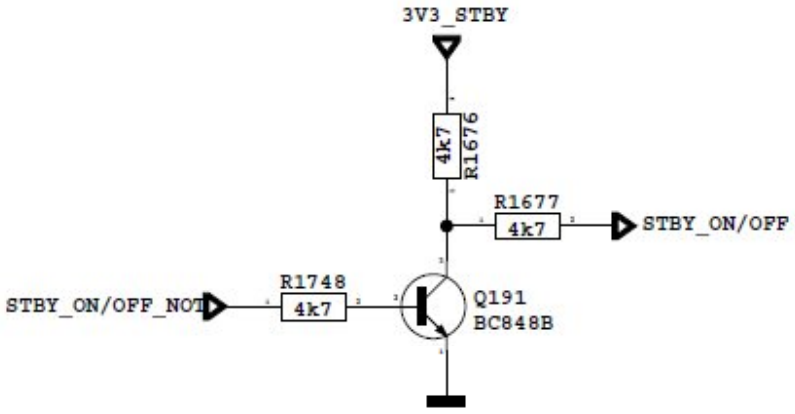
Dimming pin should be high or square wave in open position. If it is low, please check S16 for Mstar side and panel or power cables, connectors.



Backlight power supply should be in panel specs. Please check CN705 for MB81, related connectors for power supply cards.



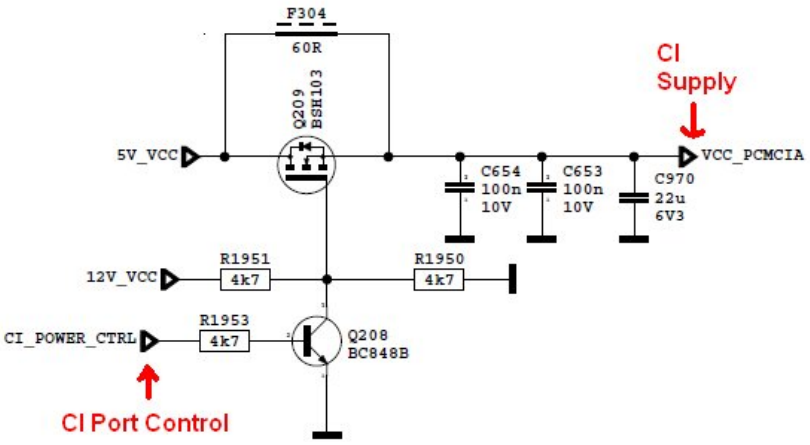
STBY_ON/OFF should be low for standby on condition, please check R1677.



14.2. CI Module Problem

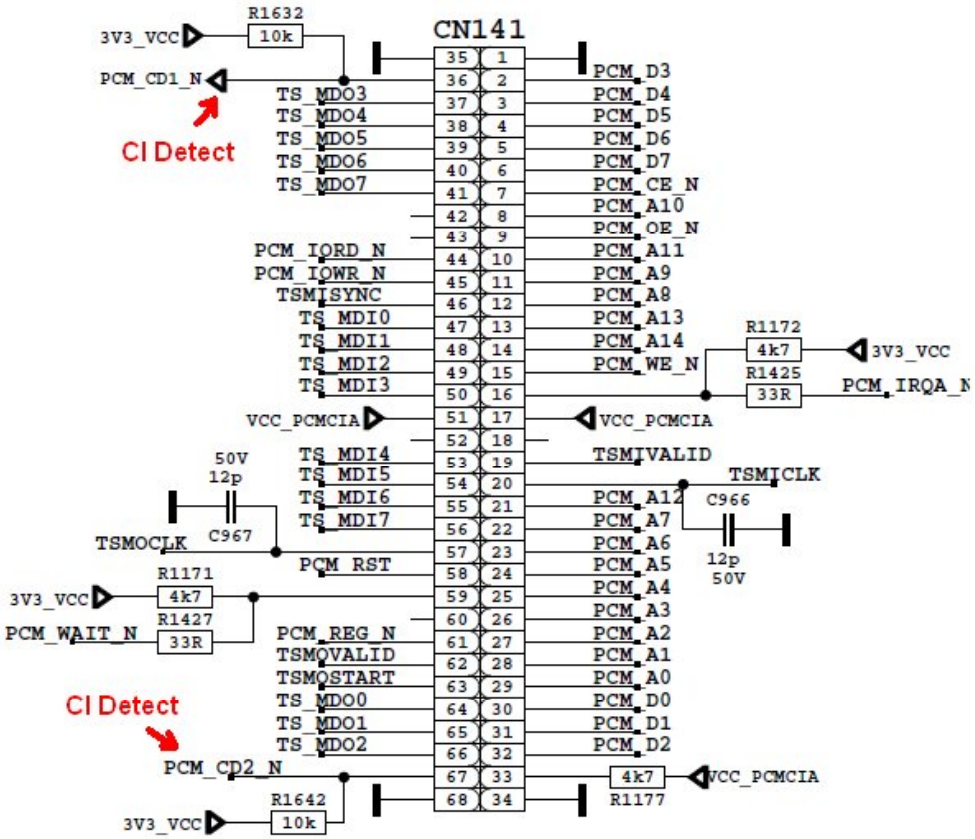
Problem: CI is not working when CI module inserted.

Possible couses: Supply, suply control pin, detect pins, mechanical positions of pins
CI supply shoul be 5V when CI module inserted. If it is not 5V please check CI_POWER_CTRL, this pin should be low.



Please check mechanical positions of CI module.

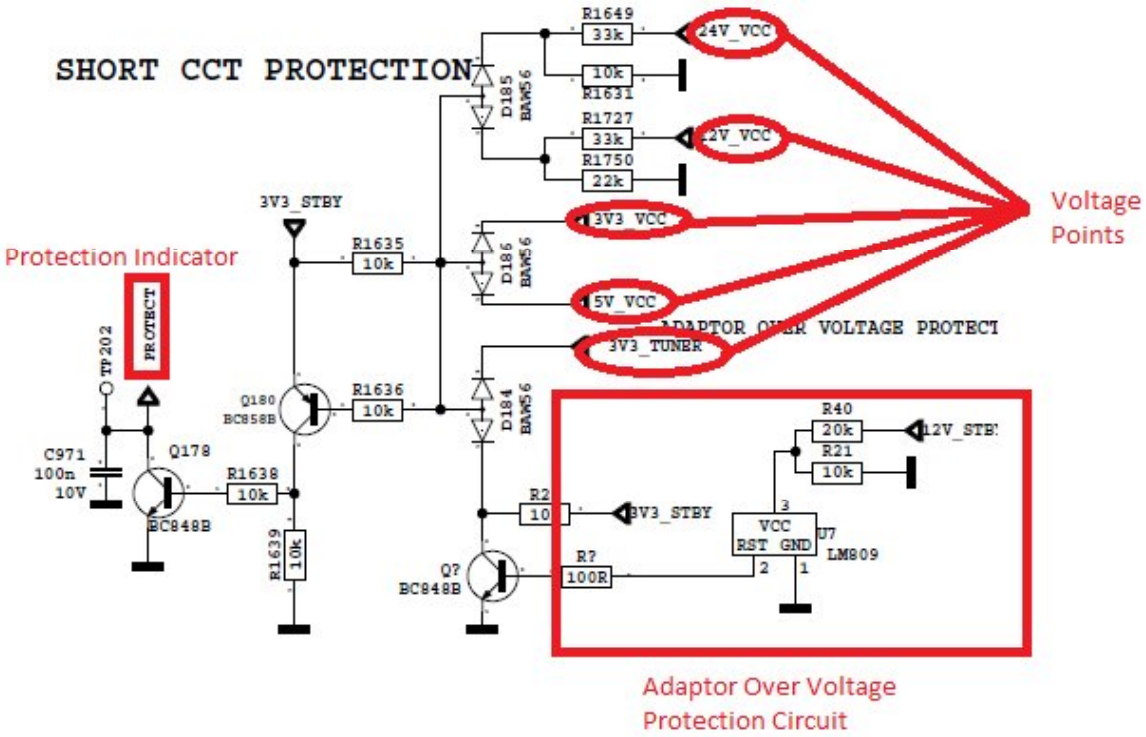
Detect ports should be low. If it is not low please check CI connector pins, CI module pins and 3V3_VCC on MB81.



14.3. Led Blinking Problem

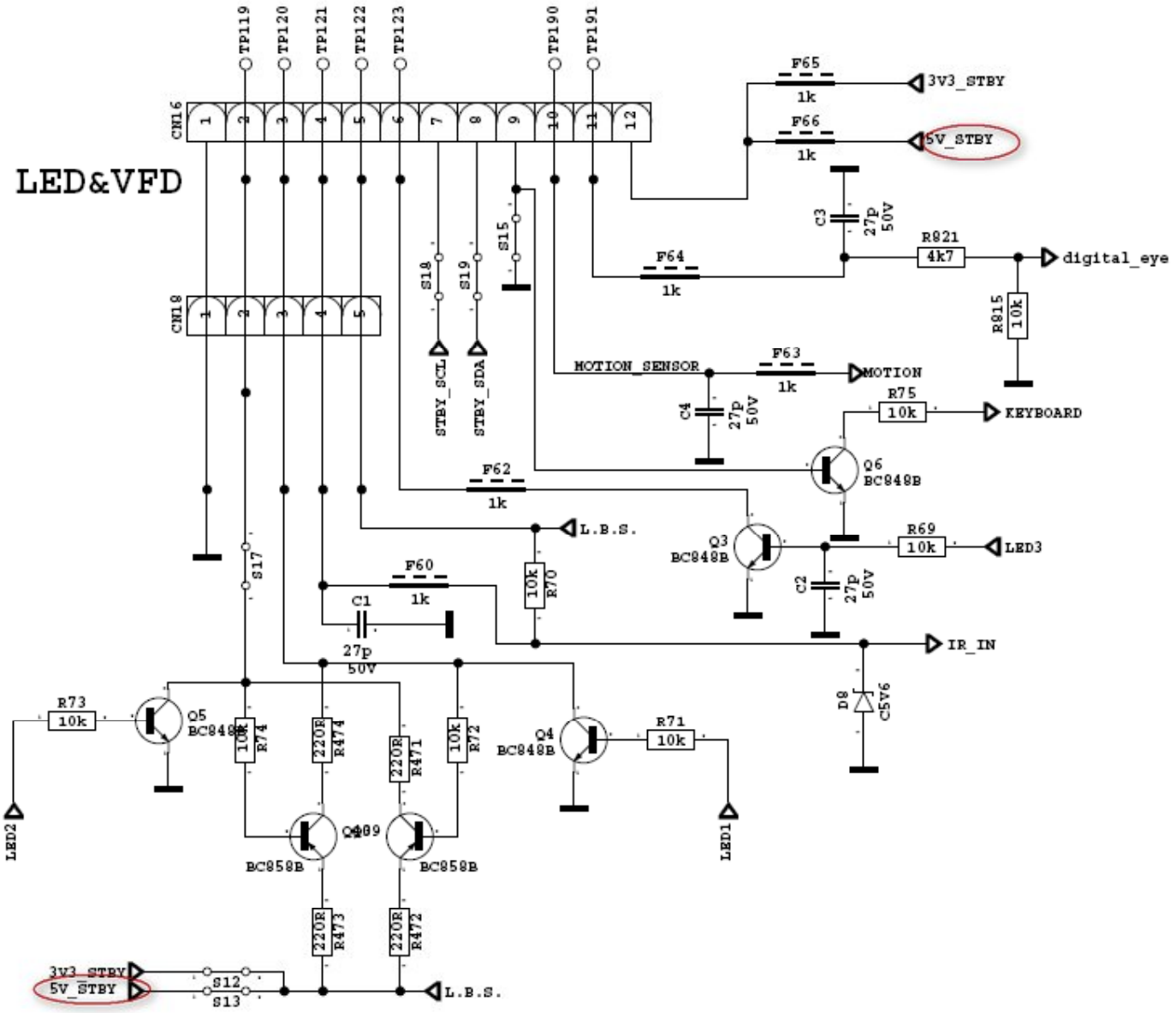
Problem: LED blinking, no other operation

This problem indicates a short on Vcc voltages. Protect pin should be logic high while normal operation. When there is a short circuit protect pin will be logic low. If you detect logic low on protect pin, unplug the TV set and control voltage points with a multimeter to find the shorted voltage to ground.



14.4. IR Problem

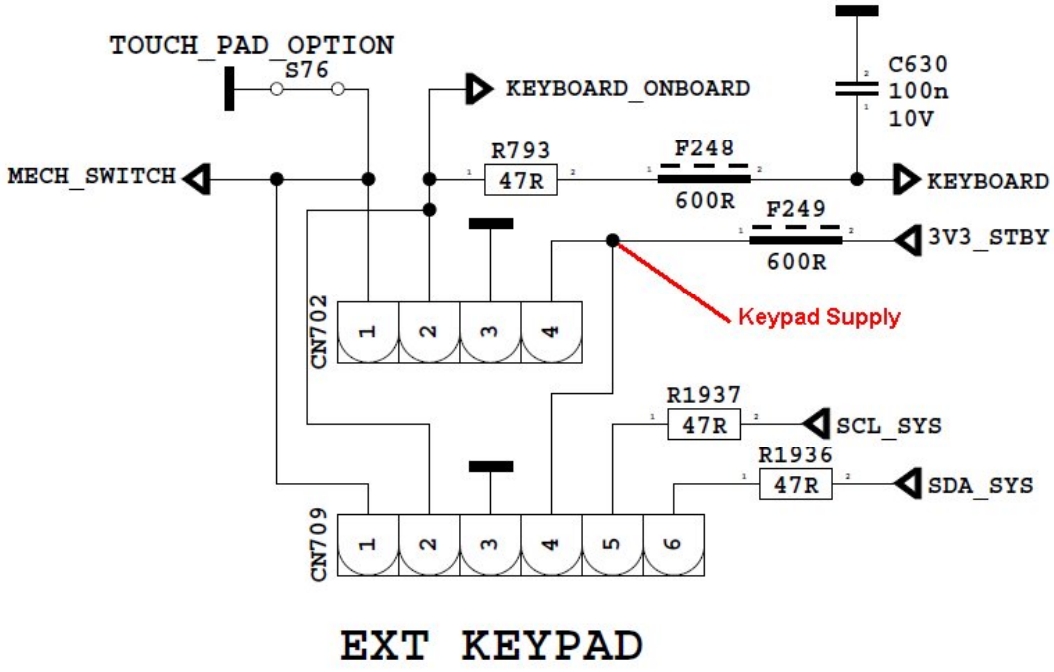
Problem: LED or IR not working
Check LED card supply on MB81 chasis.



14.5. Keypad Touchpad Problems

Problem: Keypad or Touchpad is not working

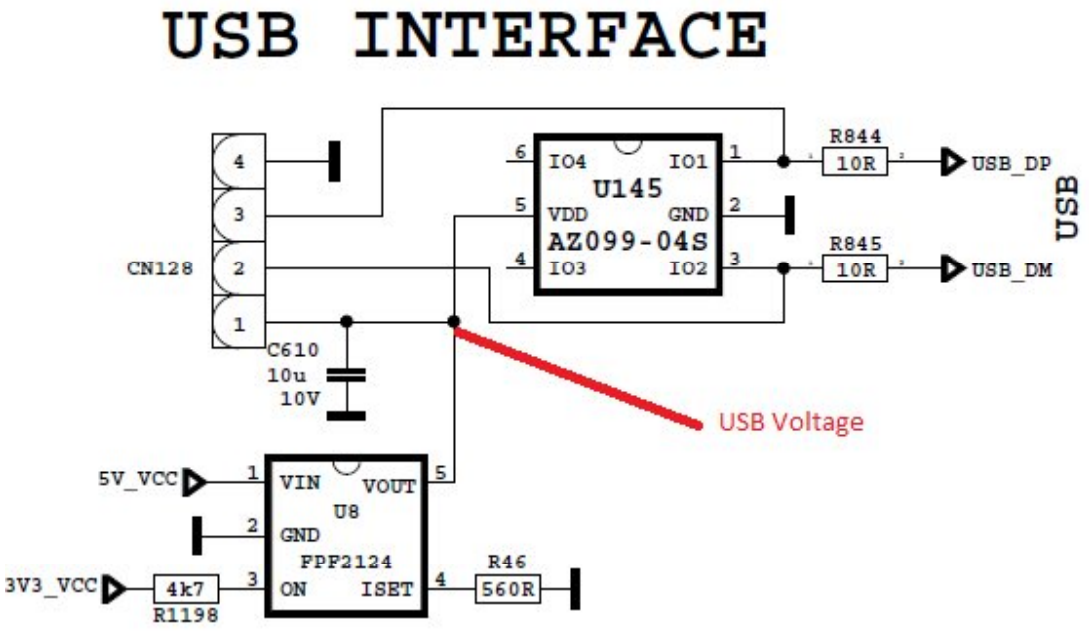
Check keypad supply and KEYBOARD pin on MB81.



14.6. USB Problems

Problem: USB is not working or no USB Detection.

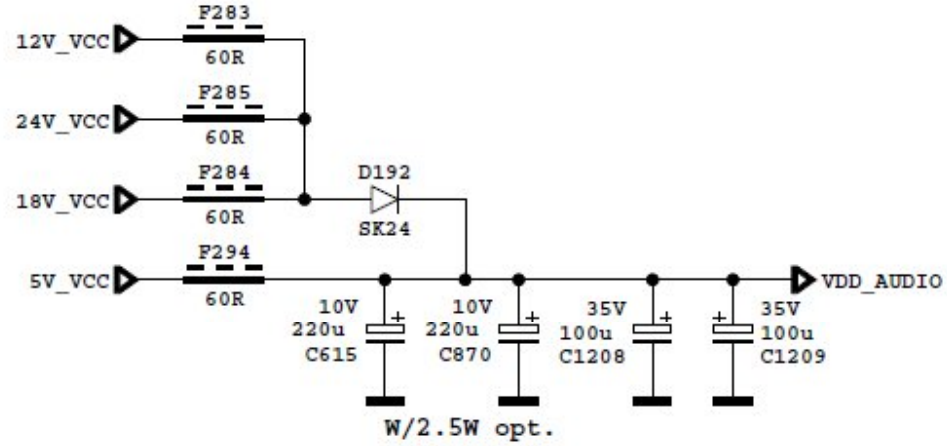
Check USB Supply, It should be nearly 5V.



14.7. No Sound Problem

Problem: No audio at main TV speaker outputs.

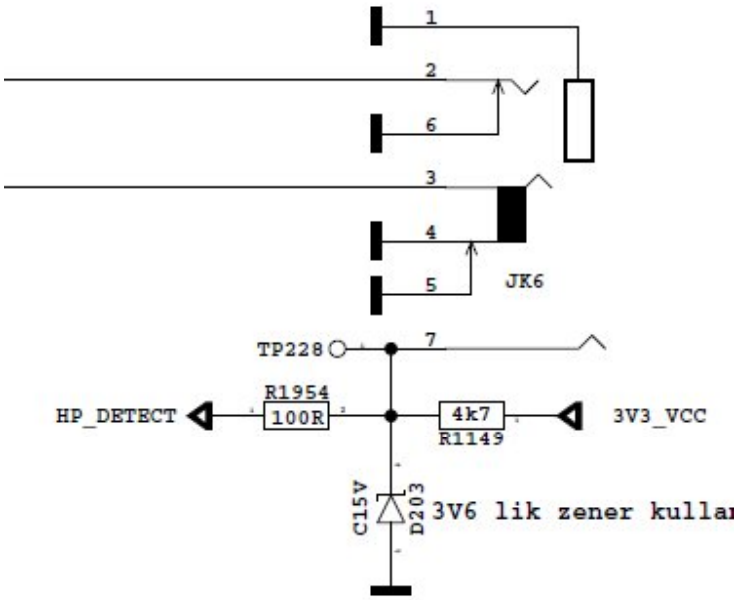
Check supply voltages of VDD_AUDIO, 5V_VCC and 3V3_VCC with a voltage-meter.
There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3v.



14.8. No Sound Problem at Headphone

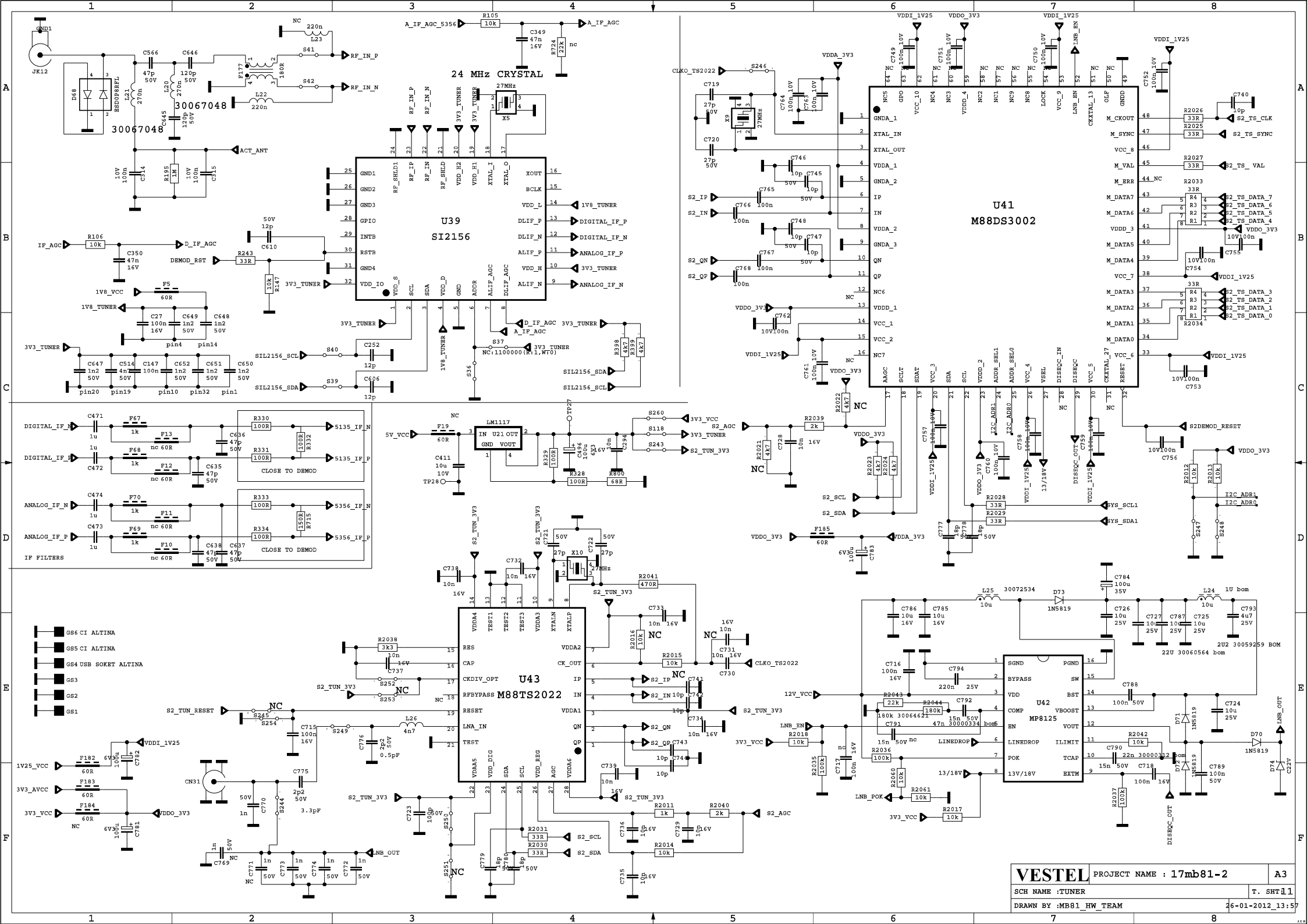
Problem: No audio at headphone output.

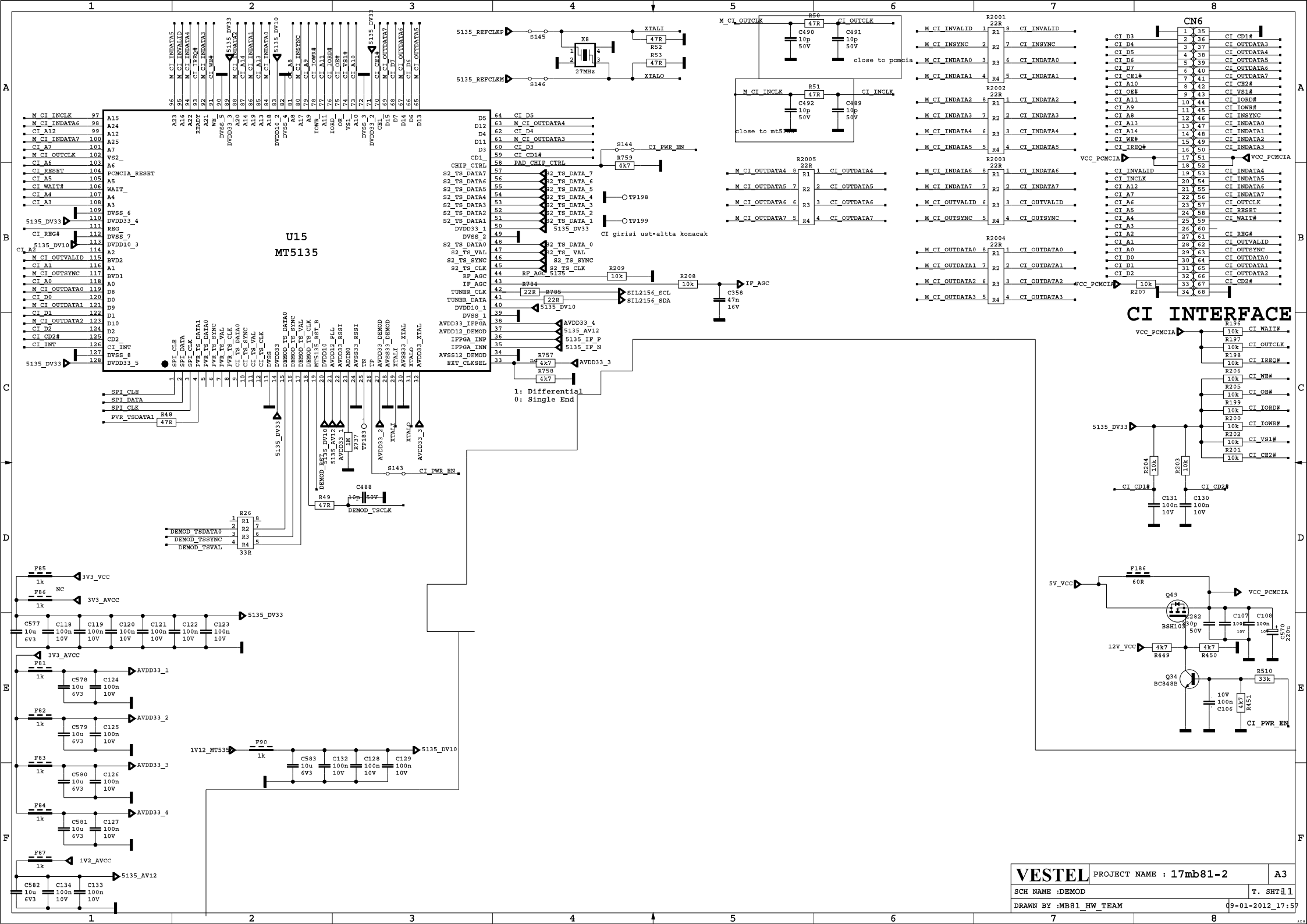
Check HP detect pin, when headphone is. Check 5V_VCC and 3V3_VCC with a voltage-meter.

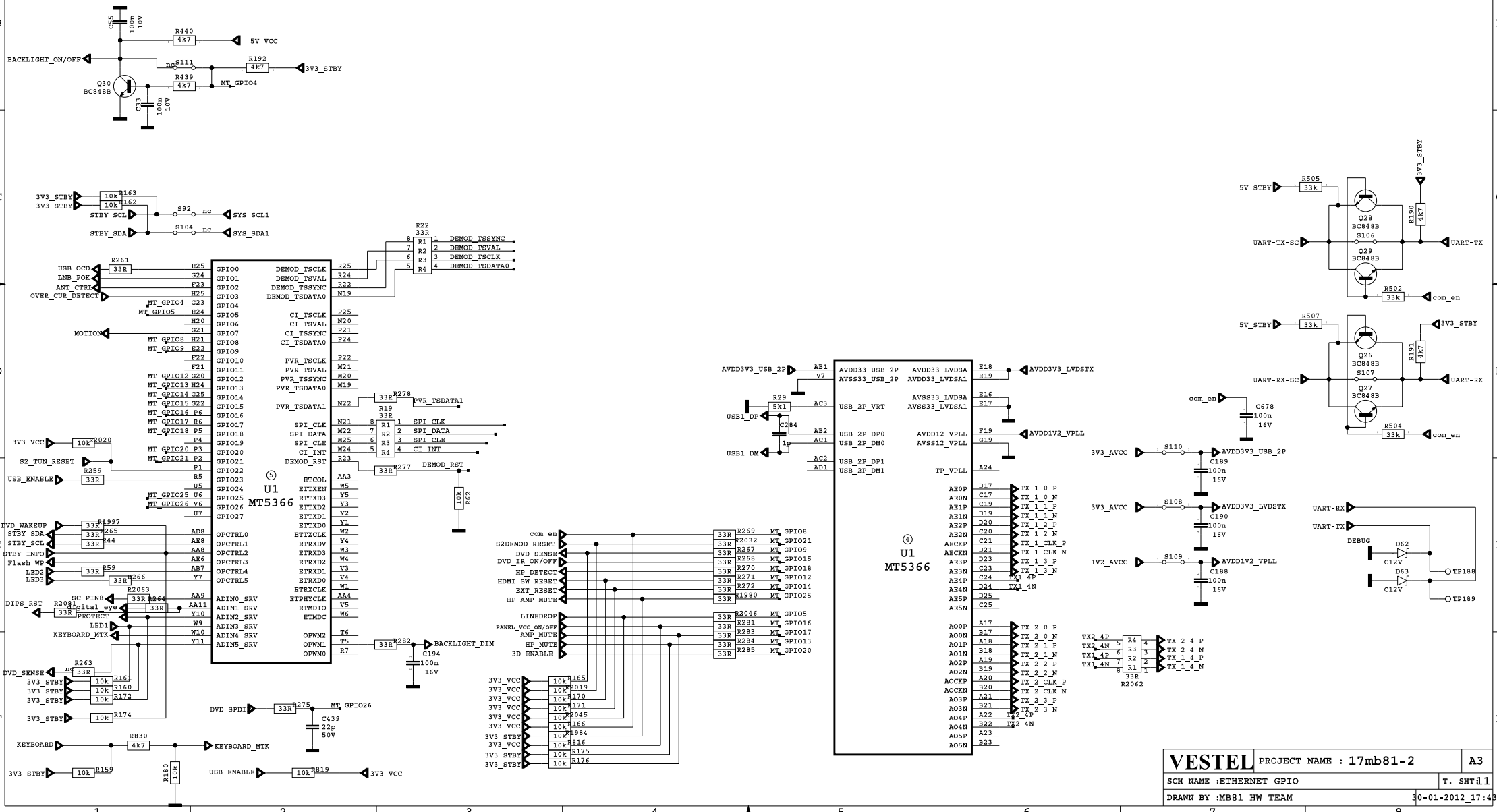


14.9. Standby On/Off Problem

Problem:
Device cannot boot, TV hangs in standby mode.

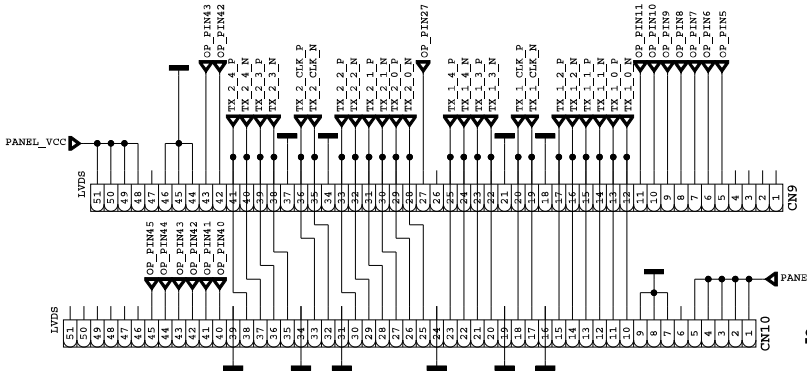

U39
SI2156
U41
M88DS3002
U43
M88TS2022
U42
MP8125
24 MHz CRYSTAL
30067048
IF FILTERS
CLOSE TO DEMOD
PROJECT NAME : 17mb81-2
SCH NAME :TUNER
DRAWN BY :MB81_HW_TEAM
26-01-2012_13:57


U15
MT5135
CI INTERFACE
CN6
1: Differential
0: Single End
CI girisi ust-altta konacak
close to pcmcia
close to mt5135
VESTEL
PROJECT NAME : 17mb81-2
A3
SCH NAME :DEMOD
T. SHT 11
DRAWN BY :MB81_HW_TEAM
09-01-2012_17:57

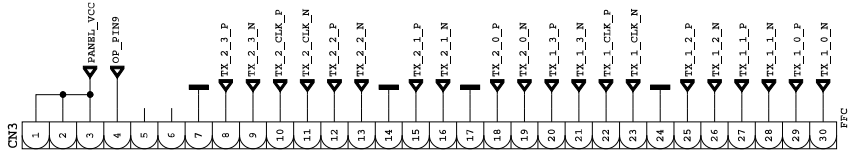


VESTEL	PROJECT NAME : 17mb81-2		A3
SCH NAME :ETHERNET_GPIO		T. SHT	11
DRAWN BY :MB81_HW_TEAM		30-01-2012_17:43	

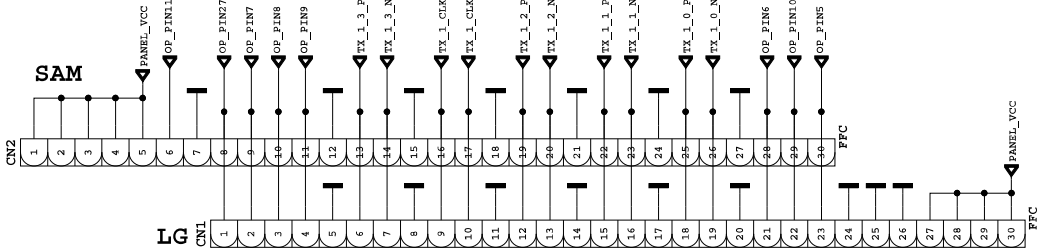
FHD 50Hz 3D FFC



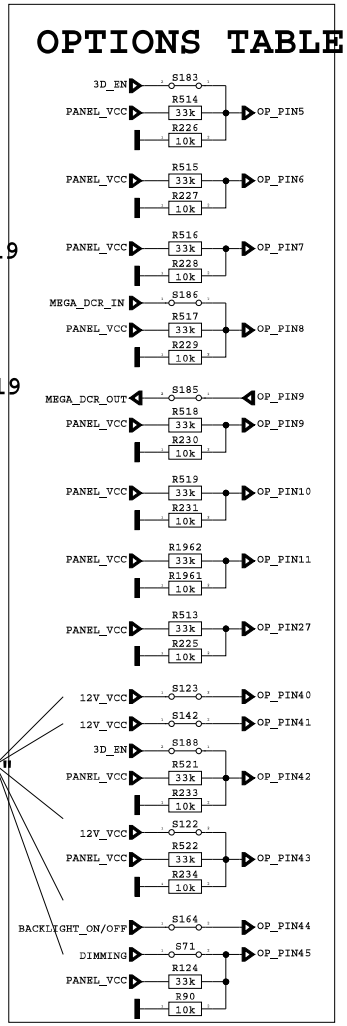
19" TO 22" DOUBLE LVDS FFC OPTIONS



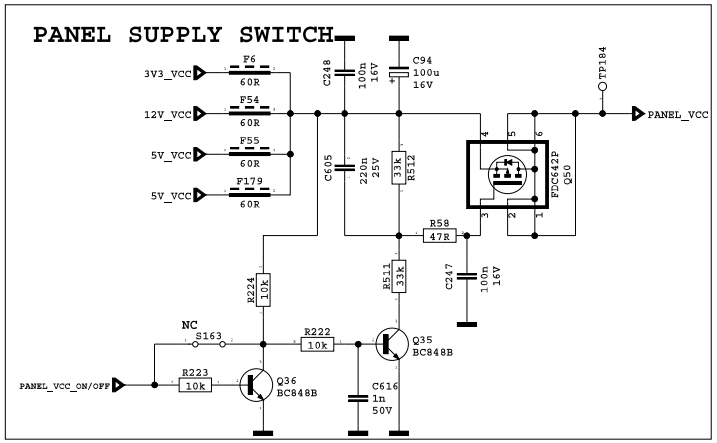
WXGA FFC

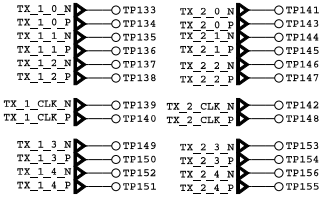


OPTIONS TABLE

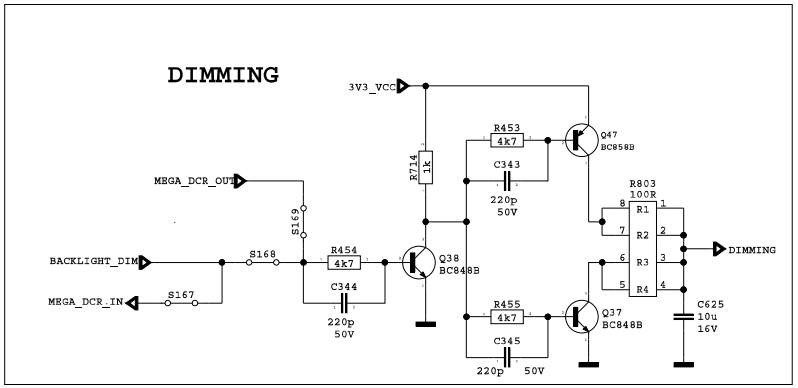


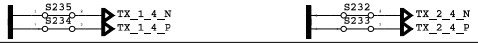
PANEL SUPPLY SWITCH



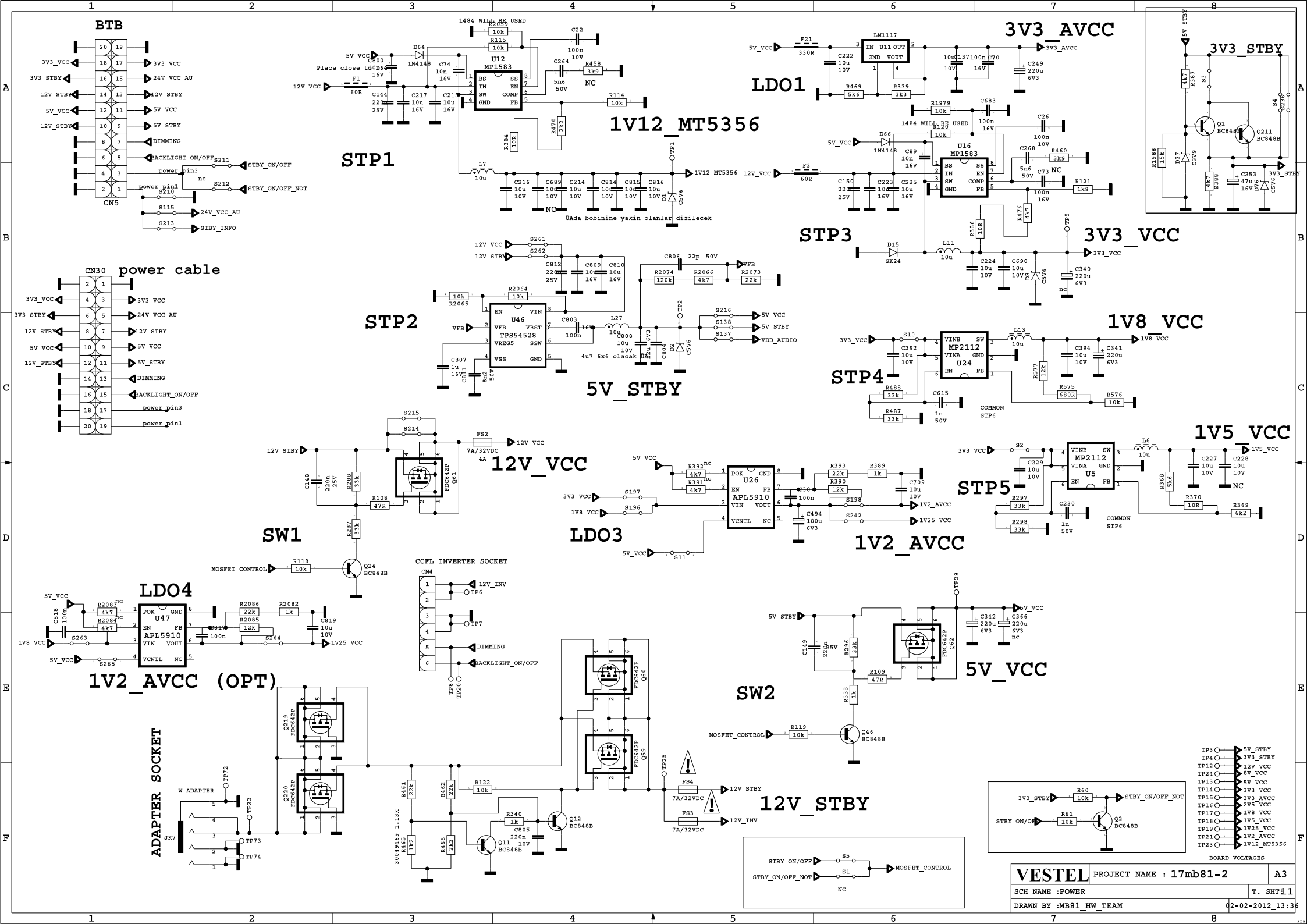


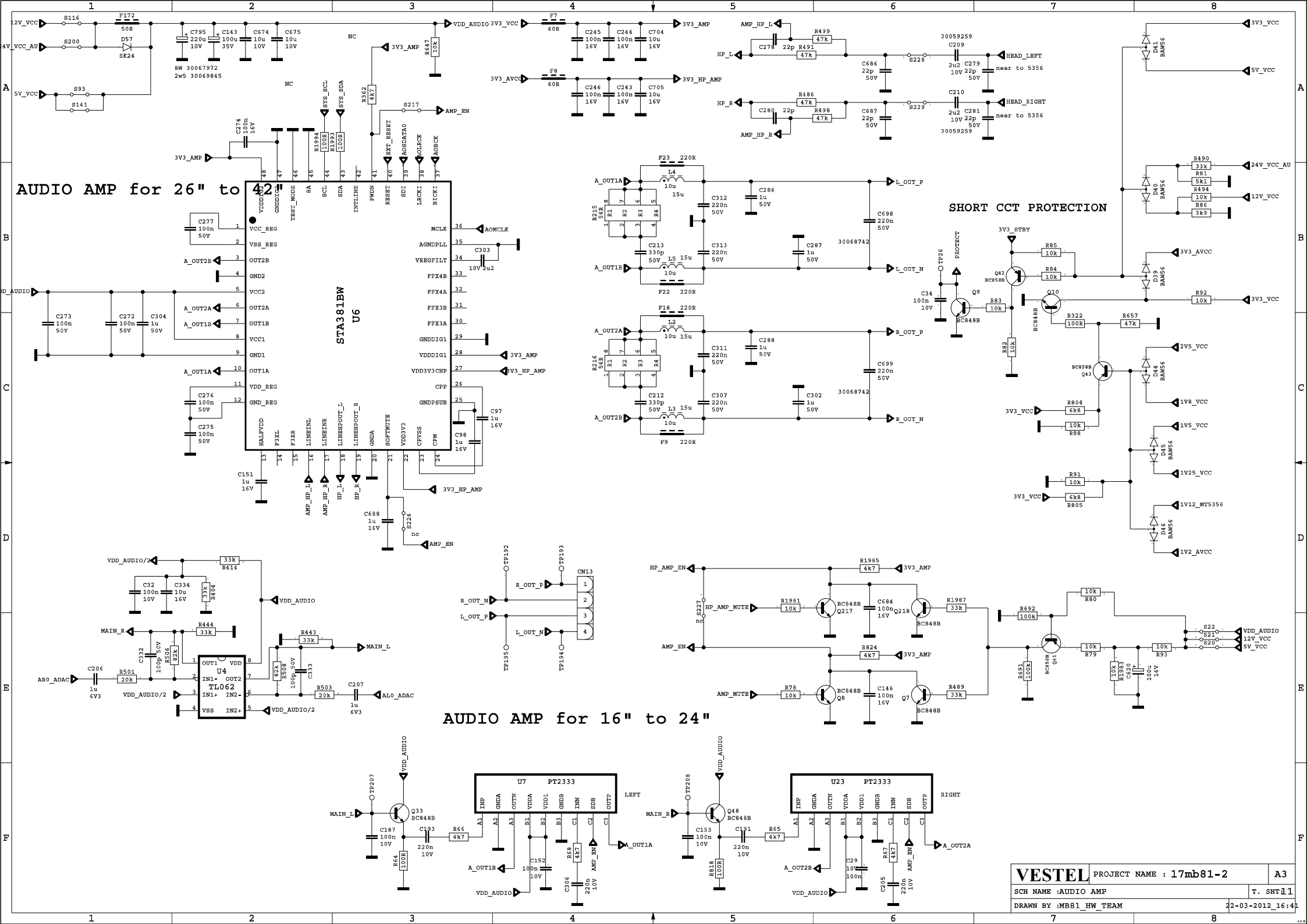
DIMMING

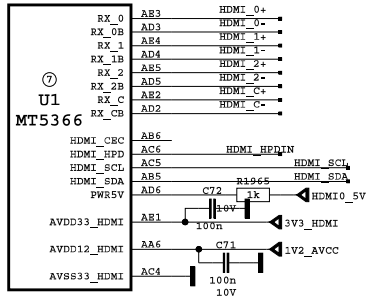


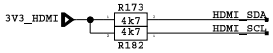


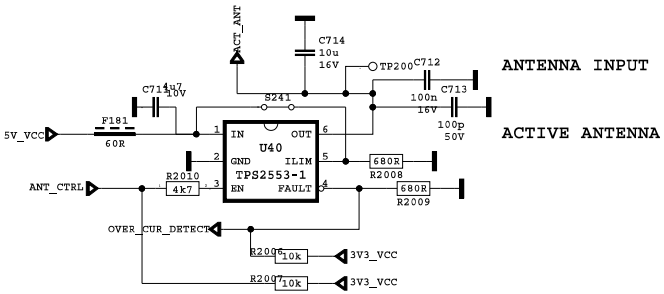
VESTEL	PROJECT NAME : 17mb81-2	A3
SCH NAME :LVDS CON		T. SHT:11
DRAWN BY :MB81_HW_TEAM		01-12-2011_13:55

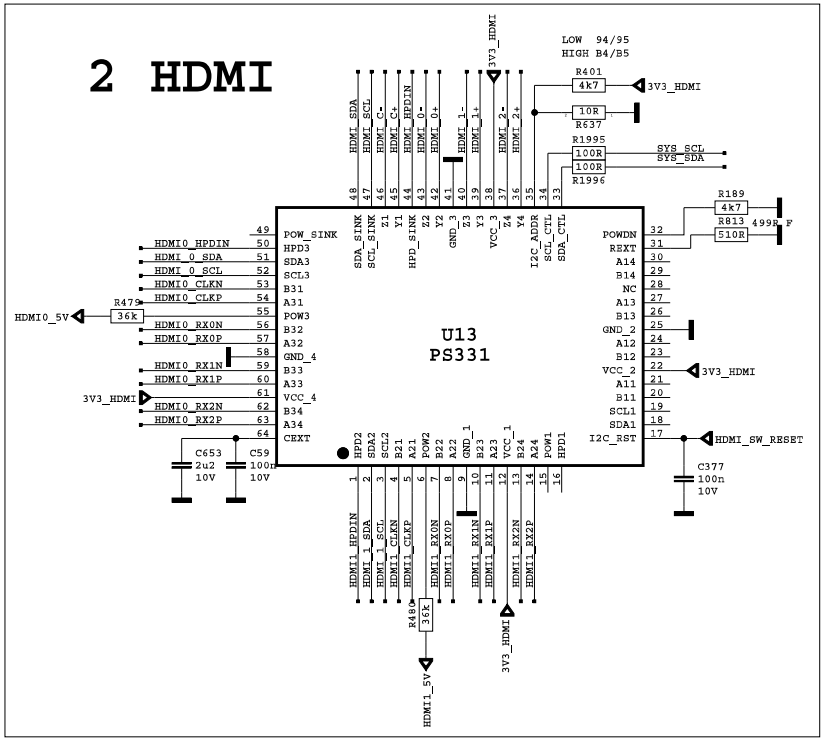

BTB
CN5
3V3_VCC
3V3_STBY
12V_STBY
5V_VCC
5V_STBY
DIMMING
BACKLIGHT_ON/OFF
power_pin3
power_pin1
STBY_ON/OFF
STBY_ON/OFF_NOT
24V_VCC_AU
STBY_INFO
1484 WILL BE USED
U12
MP1583
1V12_MT5356
STP1
ÜAda bobinine yakin olanlar dizilecek
3V3_AVCC
LDO1
LM1117
U16
STP3
1V8_VCC
U46
TPS54528
5V_STBY
STP2
power cable
CN30
U24
MP2112
STP4
COMMON
STP6
1V5_VCC
U5
STP5
12V_VCC
SW1
FS2
7A/32VDC
4A
MOSFET_CONTROL
Q24
BC848B
LDO3
U26
APL5910
1V2_AVCC
S11
LDO4
U47
1V2_AVCC (OPT)
CCFL INVERTER SOCKET
CN4
12V_INV
DIMMING
BACKLIGHT_ON/OFF
ADAPTER SOCKET
W_ADAPTER
JK7
12V_STBY
SW2
5V_VCC
Q46
BC848B
Q12
Q11
FS4
FS3
STBY_ON/OFF
STBY_ON/OFF_NOT
MOSFET_CONTROL
NC
BOARD VOLTAGES
VESTEL
PROJECT NAME : 17mb81-2
A3
SCH NAME :POWER
T. SHT:11
DRAWN BY :MB81_HW_TEAM
02-02-2012_13:36

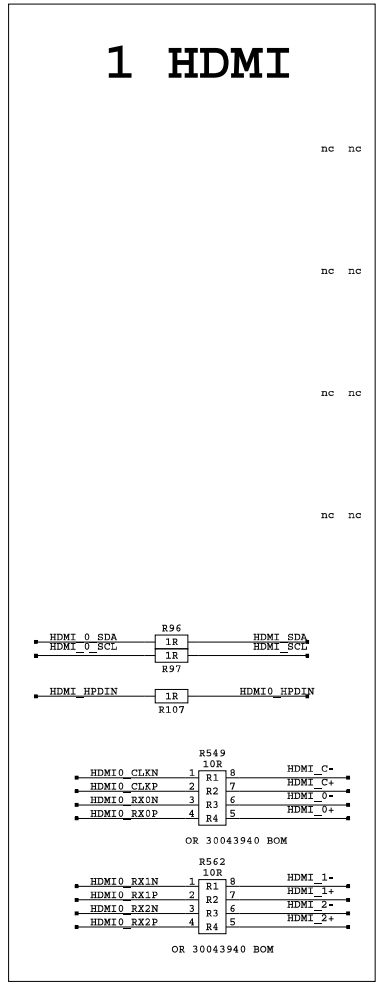

AUDIO AMP for 26" to 42"
STA381BW
U6
SHORT CCT PROTECTION
AUDIO AMP for 16" to 24"
U4
TL062
U7 PT2333
U23 PT2333
LEFT
RIGHT
VESTEL
PROJECT NAME : 17mb81-2
A3
SCH NAME :AUDIO AMP
T. SHT:1 1
DRAWN BY :MB81_HW_TEAM
22-03-2012_16:41

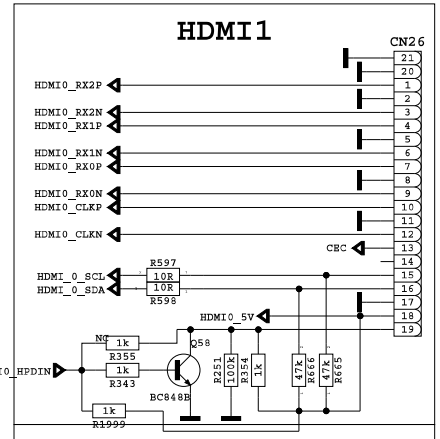


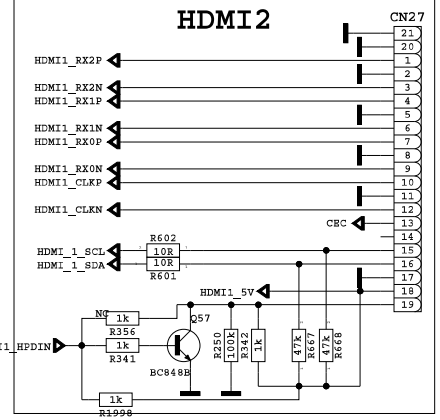


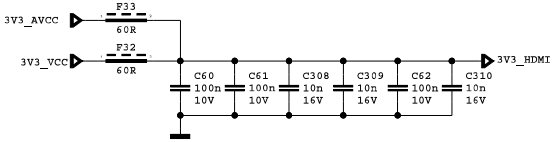




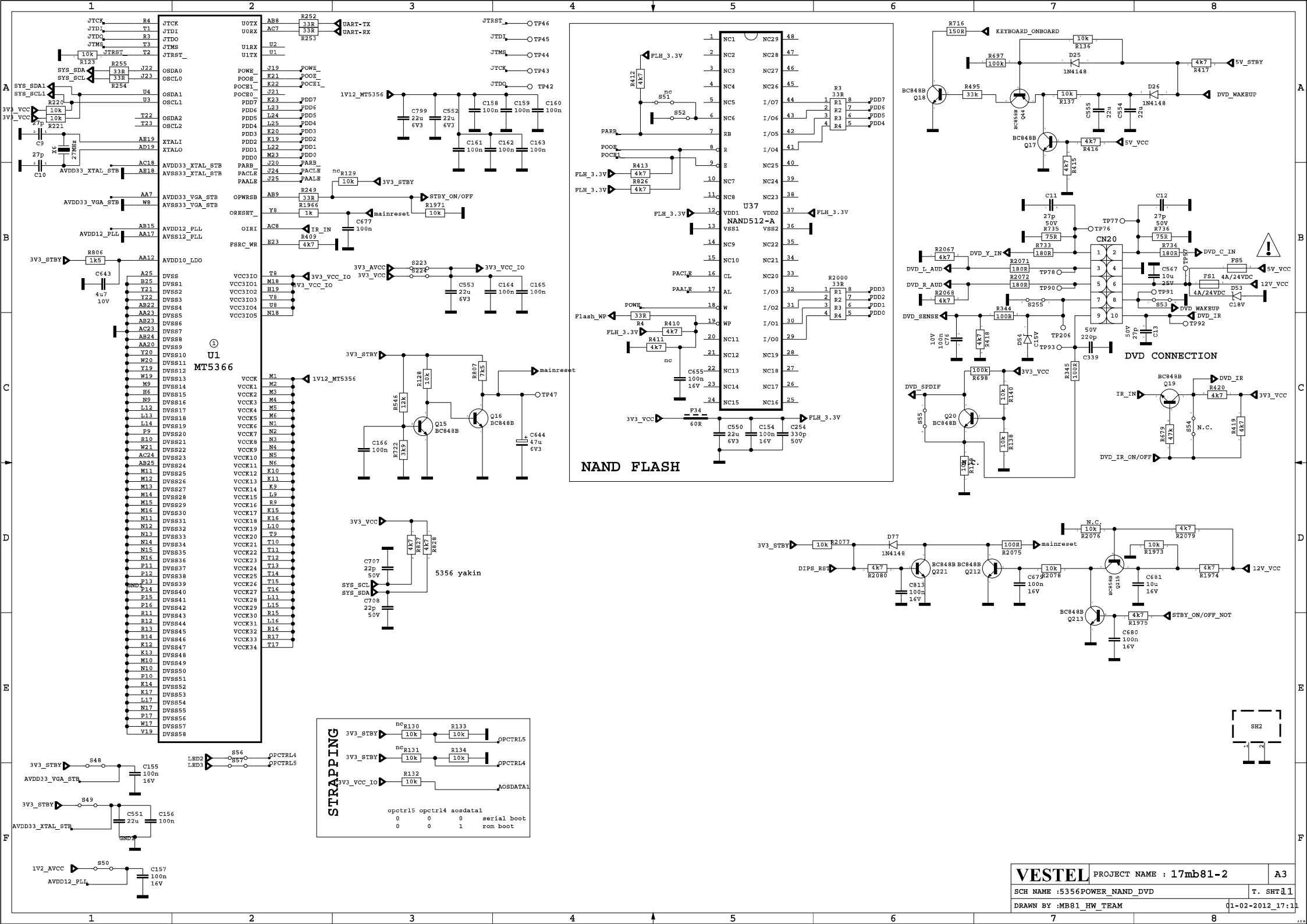


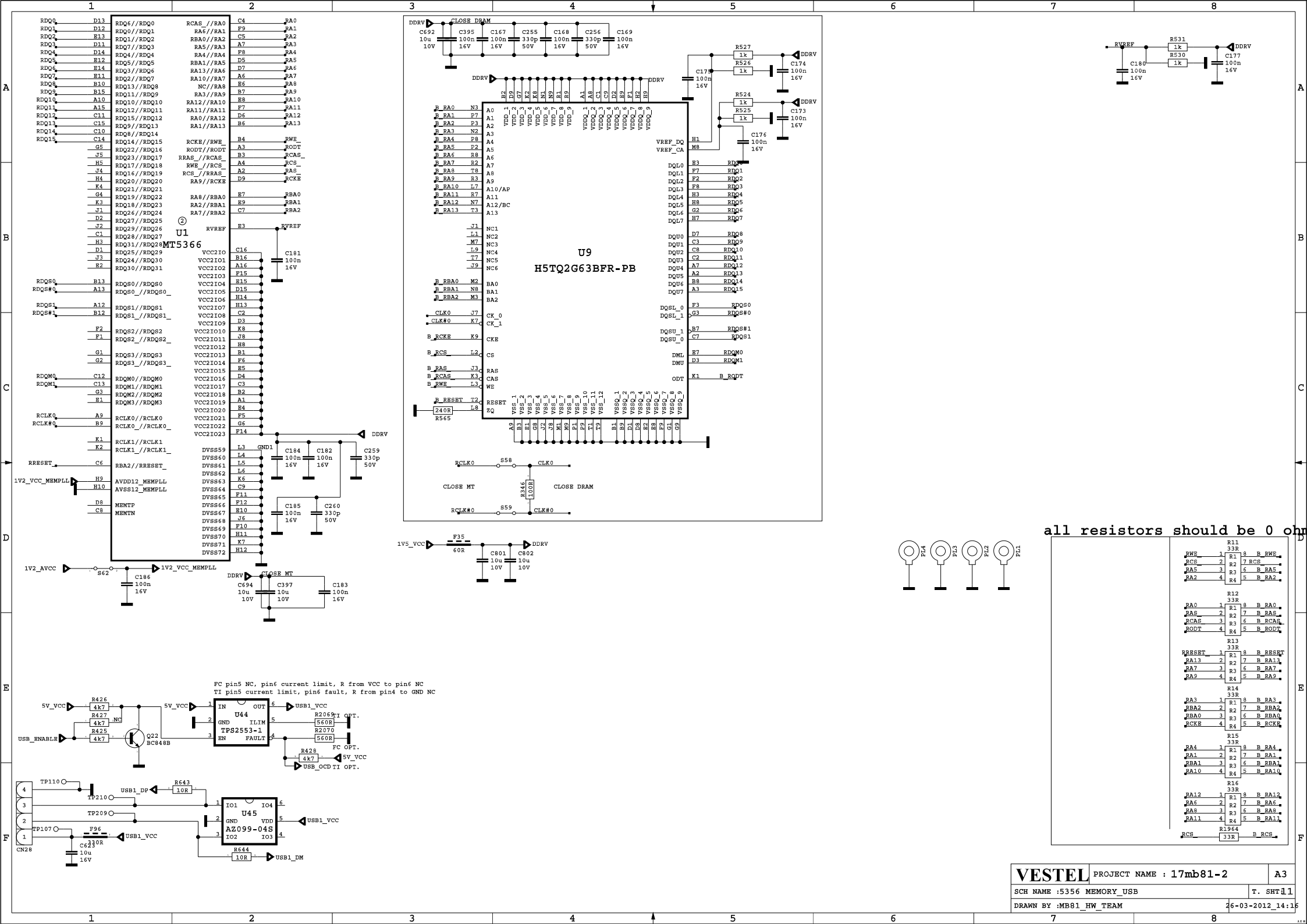




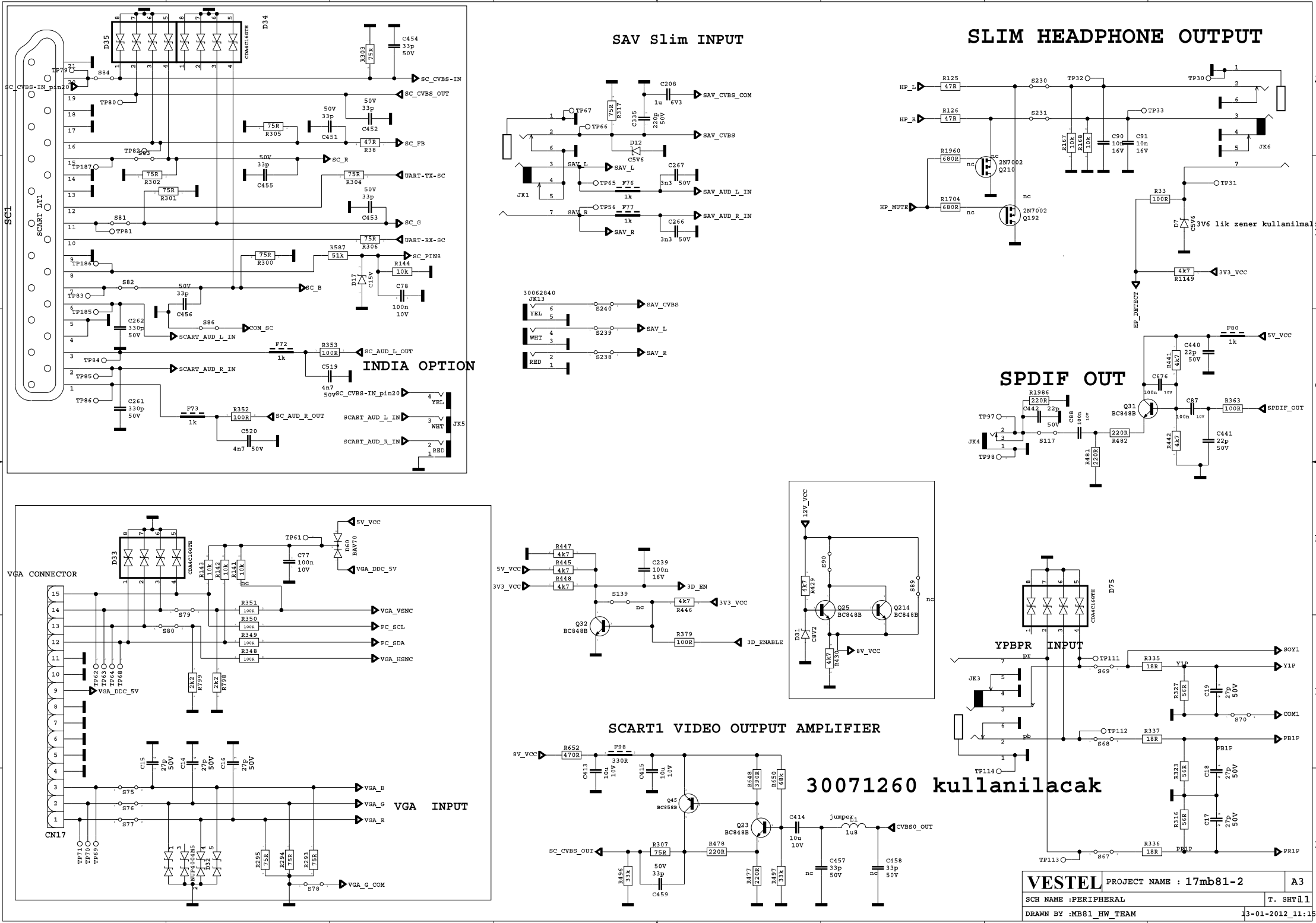


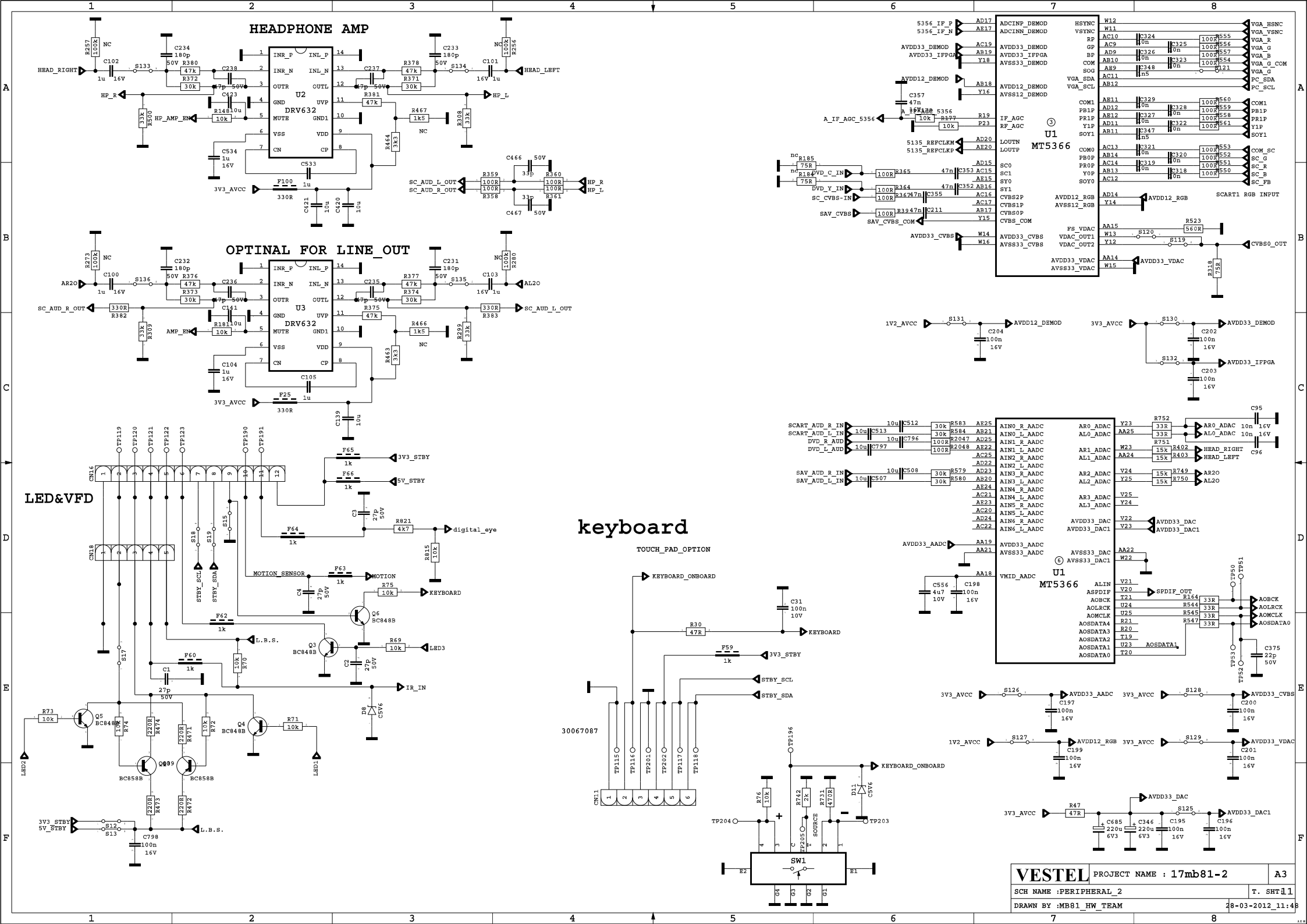
VESTEL	PROJECT NAME : 17mb81-2	A3
SCH NAME :HDMI		T. SHT: 11
DRAWN BY :MB81_HW_TEAM		12-01-2012_08:46


U1
MT5366
NAND FLASH
U37
NAND512-A
DVD CONNECTION
CN20
STRAPPING
5356 yakin
opctrl15 opctrl14 aosdata1
0 0 0 serial boot
0 0 1 rom boot
VESTEL
PROJECT NAME : 17mb81-2
A3
SCH NAME :5356POWER_NAND_DVD
T. SHT:11
DRAWN BY :MB81_HW_TEAM
01-02-2012_17:11



VESTEL	PROJECT NAME : 17mb81-2
SCH NAME :5356 MEMORY_USB	T. SHT :11
DRAWN BY :MB81_HW_TEAM	26-03-2012_14:16


SCART LT1
SC_CVBS-IN_pin20
SC_CVBS-IN
SC_CVBS_OUT
SC_FB
SC_R
UART-TX-SC
SC_G
UART-RX-SC
SC_PIN8
SC_B
COM_SC
SCART_AUD_L_IN
SC_AUD_L_OUT
SCART_AUD_R_IN
SC_AUD_R_OUT
INDIA OPTION
SAV Slim INPUT
SAV_CVBS_COM
SAV_CVBS
SAV_L
SAV_AUD_L_IN
SAV_AUD_R_IN
SAV_R
SLIM HEADPHONE OUTPUT
HP_L
HP_R
HP_MUTE
HP_DETECT
3V6 lik zener kullanilmali
3V3_VCC
SPDIF OUT
5V_VCC
SPDIF_OUT
VGA CONNECTOR
VGA_VSNC
PC_SCL
PC_SDA
VGA_HSNC
VGA_DDC_5V
VGA_B
VGA_G
VGA_R
VGA_G_COM
VGA INPUT
3D_EN
3D_ENABLE
12V_VCC
8V_VCC
SCART1 VIDEO OUTPUT AMPLIFIER
CVBS0_OUT
30071260 kullanilacak
YPBPR INPUT
SOY1
Y1P
COM1
PB1P
PR1P
VESTEL
PROJECT NAME : 17mb81-2
A3
SCH NAME :PERIPHERAL
T. SHT:11
DRAWN BY :MB81_HW_TEAM
13-01-2012_11:15


HEADPHONE AMP
OPTINAL FOR LINE_OUT
LED&VFD
keyboard
TOUCH_PAD_OPTION
U1
MT5366
U2
DRV632
U3
DRV632
SCART1 RGB INPUT
VESTEL
PROJECT NAME : 17mb81-2
A3
SCH NAME :PERIPHERAL_2
T. SHT:11
DRAWN BY :MB81_HW_TEAM
28-03-2012_11:48