MB230 IDTV
SERVICE MANUAL

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IMPORTANT

Before removing the rear cover from the TV for servicing, make sure that no cables are fixated to the cover. Release the cables from their clamps and disconnect (if any). Failure to do so may damage the wires and/or other components of the TV.

1. INTRODUCTION

17MB230 main board is driven by Novatek SOC. This IC is a single chip iDTV solution which compliants with variety ATV as NTSC, PAL and SECAM, and DTV standards as ISDB-T, DVB-T/-T2/-C/-S/-S2/-S2X, ITU-T J.83B, 8VSB, DTMB, integrates DTV and multi-media AV decoder, SIF demodulator, and support A/V post-processing.

Key features include:

- DTMB, DVB-T,T2,DVB-C, DVB-S/S2/S2X demodulators
- A multi standart A/V format decoder
- 5th generation Advanced Scaling Up Engine
- Embedded dual 10 bit LVDS transmitter
- Dedicated dual DSP to decode compressed audio and post-processing
- 4K2K 60p HDMI input
- Mılti-purpose CPU for OS and multimedia
- Peripheral and power management
- Embedded DRAM

Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF
- 1 Satellite input
- 1 Side AV (CVBS, R/L_Audio)
- 1 BAV-IN socket(Common)
- 1 PC input(Common)
- 4 HDMI input
- 1 Common interface(Common)
- 1 Optic/ Quax S/PDIF output
- 1 Headphone(Common)
- 2 USB(1x common, 1x optional) and 2x internal USB for Wifi/Bluetooth
- 1 Ethernet-RJ45
- 1 External Touchpad/ Keyboard/Magic Button

2. T/T2/C/A TUNER (U1)

Description

The MxL661 is a highly integrated low-power silicon tuner IC that targets all global and digital cable standards. Broadband input filtering and channel filtering have been completely integrated on-chip. This integration enables a compact design resulting in small footprint, low Bill-Of-Material (BOM) cost, and low-power consumption.

A signal at the 75ohm RF input is filtered and converted to a programmable IF output frequency. Automatic Gain Control (AGC), LO generation, and channel selectivity functions are completey integrated on the chip. All functions of the IC can be controlled using the I2C interface.

The MxL is available in a 4 mm x 4mm x 0.85mm3, 24-pin QFN package.

Features

- Tuning range from 44MHz to 1002MHz
- Programmable channel bandwidths of 6, 7, and 8MHz
- Integrated channel filtering
- Low power consumption with 3.3V and 1.8V dual-supply operation - 351 mW (digital terrestrial)
- On-chip voltage regulator enables single supply 3.3V operation
- Programmable IF frequency and IF spectrum inversion
- Programmable RF to IF delay for ATV scrambling systems that relies on the H-Sync method
- Optioanl balun-less application note for cost-sensitive applications
- Reference clock output available for re-use by demodulators and additional tuners in multi-channel applications
- Input power reporting
- Open-drain General Purpose Output GPO available for controlling off-chip circuitry
- I^2C compatible digital control interface
- RoHS compliance

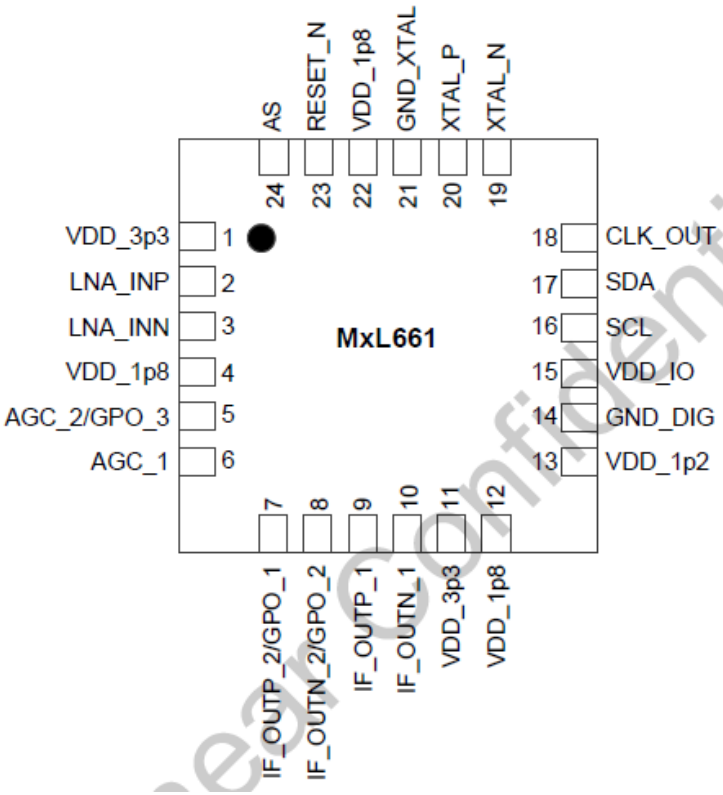


Figure 1 Pin description

Pin #	Pin Name
1	VDD_3p3
2	LNA_INP
3	LNA_INN
4	VDD_1p8
5	AGC_2/GPO_3
6	AGC_1
7	IF_OUTP_2/GPO_1
8	IF_OUTN_2/GPO_2
9	IF_OUTP_1
10	IF_OUTN_1
11	VDD_3p3
12	VDD_1p8

Pin #	Pin Name
13	VDD_1p2
14	GND_DIG
15	VDD_IO
16	SCL
17	SDA
18	CLK_OUT
19	XTAL_N
20	XTAL_P
21	GND_XTAL
22	VDD_1p8
23	RESET_N
24	AS

Table 1 Pin functions

3. S/S2 TUNER (U142)

Description

The AV2018 is a highly integrated silicon tuner for DVB-S2 standard. It integrates a synthesizer, crystal oscillator, LDO, loop through path, and a direct conversion receiver including LNA, RF variable gain amplifiers, Mixer, programmable channel filter, and PGA.

The low noise figure of the receiver and loop through path eliminates the need of an external LNA. The integrated crystal oscillator can provide a reference clock for demodulator. The LDO supplies all the internal blocks the only an external voltage source is required. The AV2018 requires only a small number of external components, thus enables very competitive design.

The AV2018 implements an automatic gain control mechanism that only an analog control signal from the demodulator is required to from a close-loop gain control. The mechanism will arrange the gain of the receiver blocks to achieve best performance according to the control signal voltage. The embedded automatic calibration mechanism provides precise control of channel filter bandwidth and DC offset, no additional calibration procedure is required.

Features

- Input RF Frequency: 950Mhz to 2150Mhz
- Single +3.3V power Supply
- Embedded LNA, Mixer, VCO, crystal oscillator, and LDO
- Low Noise Figure: 5 dB, typical
- Embedded DC offset Cancellation Circuit
- Programmable channel filter with bandwith from 4MHz to 40MHz
- Automatic gain control
- Embedded RF signal loop through path
- Single-ended I/Q interface
- QFN3*3mm 16pin package

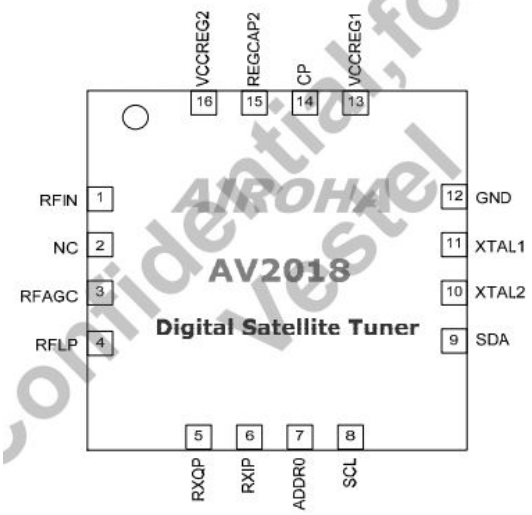


Figure 2 Pin Assigment

Confidential, for Vestel

PIN	SIGANL	TYPE	DESCRIPTION
1	RFIN	Input, Analog	RF Signal Input
2	NC	-	No Connect
3	RFAGC	Input, Analog Control	RF AGC Control Voltage
4	RFLP	Output, Analog	RF Loop Through Signal Output
5	RXQP	Output, Analog	BB Output
6	RXIP	Output, Analog	BB Output
7	ADDR0	Digital	Device Address Control
8	SCL	Input, Digital	Serial Interface
9	SDA	Input/Output, Digital	Serial Interface
10	XTAL2	Analog	XTAL Input
11	XTAL1	Analog	XTAL Input
12	GND	Ground	Ground
13	VCCREG1	VCC Supply	3.3V Supply Voltage for Regulator
14	CP	Analog	Charge Pump
15	REGCAP2	Analog	Regulator Output for External Capacitor
16	VCCREG2	VCC Supply	3.3V Supply Voltage for Regulator

Table 2 Pin Description

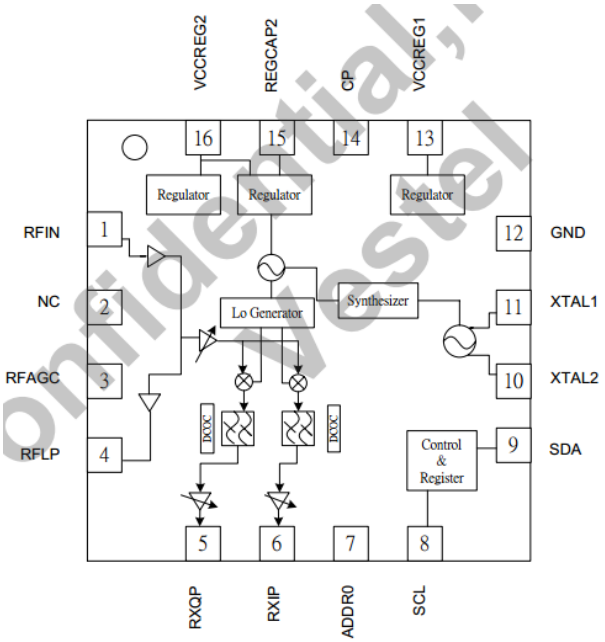


Figure 3 Functional Block Diagram

Confidential for Vestel

ITEM	MIN.	MAX.
Power supply voltage (VCCREG1/2)	– 0.3V	4.0V
Pin voltage	– 0.3V	HOST_IO_VCC + 0.3V
Maximum power dissipation	-	0.5W
Operating temperature	– 20°C	+85°C
Storage temperature	– 65°C	+150°C
LNA input level	-	+10dBm
Digital pin	-	+5mA
RFAGC pin	-	+5mA

Table 3 Absolute Maximum Ratings

4. AUDIO AMPLIFIER STAGES

A. MAIN AMPLIFIER (U9)(6-8-10 W OPTION)

Description

AD82587D is a digital audio amplifier capable of driving a pair of 8 ohm, 20W or a single 4ohm, 40W speaker, both which operate with play music at a 24V supply without external heat-sink or fan requirement.

Using I^2C digital control interface, the user can control AD82587D's input format selection, mute and volume control functions. AD82587D has many built-in protection circuits to safeguard AD82587D from connection errors.

Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting) Loudspeaker: 97dB (PSNR), 105dB (DR) @ 24V
- Multiple sampling frequencies (Fs)
  - 32kHz / 44.1kHz / 48kHz and
  - 64kHz / 88.2kHz / 96kHz and
  - 128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x,1024x Fs
  - 256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  - 128x~512x Fs for 64kHz / 88.2kHz / 96kHz
  - 64x~256x Fs for 128kHz /176.4kHz/192kHz
- Supply voltage
  - 3.3V for digital circuit
  - 10V~26V for loudspeaker driver
- Loudspeaker output power for Stereo@ 24V
  - 10W x 2ch into 8_ @ 0.16% THD+N

- 15W x 2ch into 8_ @ 0.18% THD+N
- 20W x 2ch into 8_ @ 0.24% THD+N

- Loudspeaker output power for Mono@ 24V
  - 20W x 1ch into 4_ @ 0.17% THD+N
  - 30W x 1ch into 4_ @ 0.2% THD+N
  - 40W x 1ch into 4_ @ 0.24% THD+N
- Sounds processing including:
  - Volume control (+24dB~-103dB, 0.125dB/step)
  - Dynamic range control
  - Power clipping
  - Channel mixing
  - User programmed noise gate with hysteresis window
  - DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I2C control interface with selectable device address
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage
- detection
- Power saving mode
- Dynamic temperature control

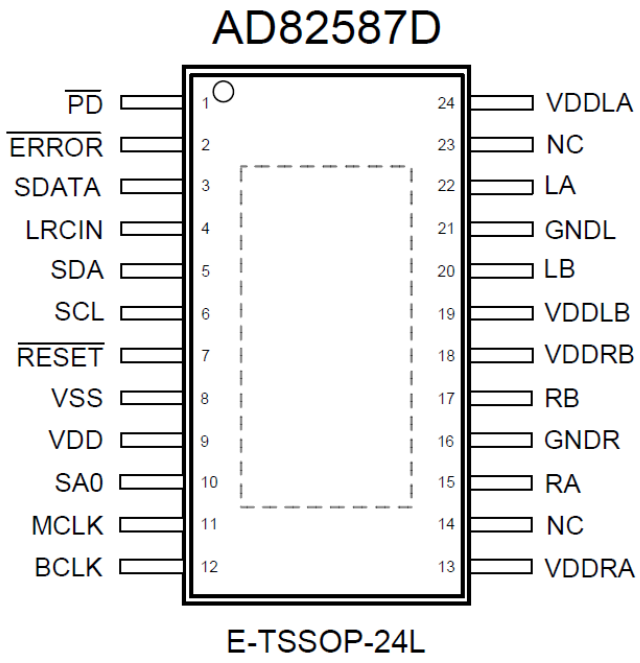


Figure 4 Pin description

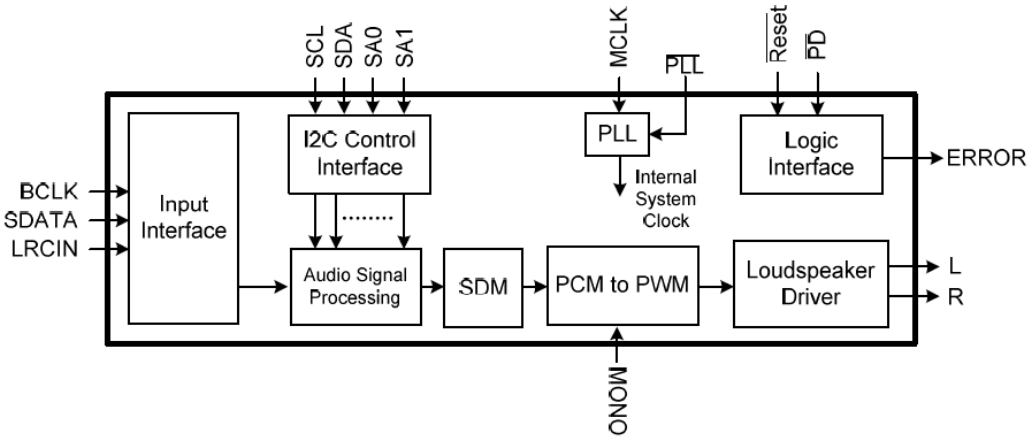


Figure 5 Functional Block Diagram

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

Table 4 Absolute Maximum Ratings

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~26	V
T_J	Junction Operating Temperature	0~125	°C
T_A	Ambient Operating Temperature	0~70	°C

Table 5 Recommended Operating Conditions

B. SUBWOOFER AMPLIFIER (U8) (12 W)

Description

AD82586C is a digital audio amplifier capable of driving a pair of 8 ohm, 20W operating at 24V supply without external heat-sink or fan requirement with play music.

AD82586C has 20 bands EQ function and can operate 20W stereo or 40W mono optionally.

AD82586C can provide advanced audio processing capabilities, such as volume control, 20 bands speaker EQ, audio mixing, 3D surround and DRC (dynamic range control). These functions are fully programmable via a simple I2C control interface.

Robust protection circuits are provided to protect AD82586C from damage due to accidental erroneous operating condition. AD82586C is more tolerant to noise and PVT (Process, Voltage, and Temperature) variation than the analog Class-AB or Class-D audio amplifier counterpart implemented by analog circuit design. AD82586C is pop free during instantaneous power switch because of its built-in, robust anti-pop circuit.

Features

- 16/18/20/24-bits input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR (A-weighting) Loudspeaker: 99dB (PSNR), 104dB (DR) @24V
- Multiple sampling frequencies (Fs)
  - 32kHz / 44.1kHz / 48kHz and
  - 64kHz / 88.2kHz / 96kHz and
  - 128kHz / 176.4kHz / 192kHz
- System clock = 64x, 128x, 192x, 256x, 384x, 512x, 576x, 768x, 1024x Fs
  - 64x~1024x Fs for 32kHz / 44.1kHz / 48kHz
  - 64x~512x Fs for 64kHz / 88.2kHz / 96kHz
  - 64x~256x Fs for 128kHz / 176.4kHz / 192kHz
- Supply voltage
  - 3.3V for digital circuit
  - 10V~26V for loudspeaker driver
- Loudspeaker output power at 24V
  - 10W x 2CH into 8 ohm @0.17% THD+N for stereo
  - 20W x 2CH into 8 ohm @0.26% THD+N for stereo
- Sound processing including:
  - 20 bands parametric speaker EQ
  - Volume control (+24dB~-103dB, 0.125dB/step)
  - Dynamic Range Control (DRC)
  - Dual band DRC
  - Power clipping
  - 3D surround sound
  - Channel mixing
  - Noise gate with hysteresis window
  - Bass/Treble tone control
  - DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I^2C control interface with selectable device address
- Support hardware and software reset
- Internal PLL
- LV Under-Voltage shutdown and HV Under-Voltage detection
- Power saving mode

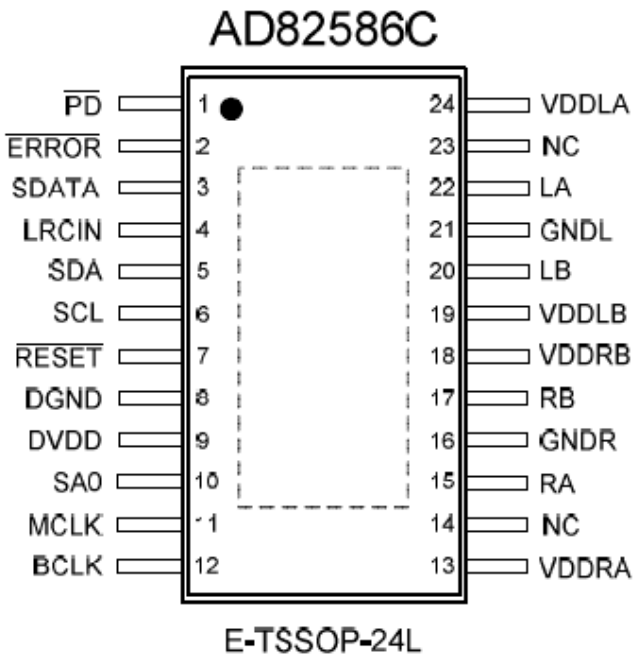


Figure 6 Pin Description

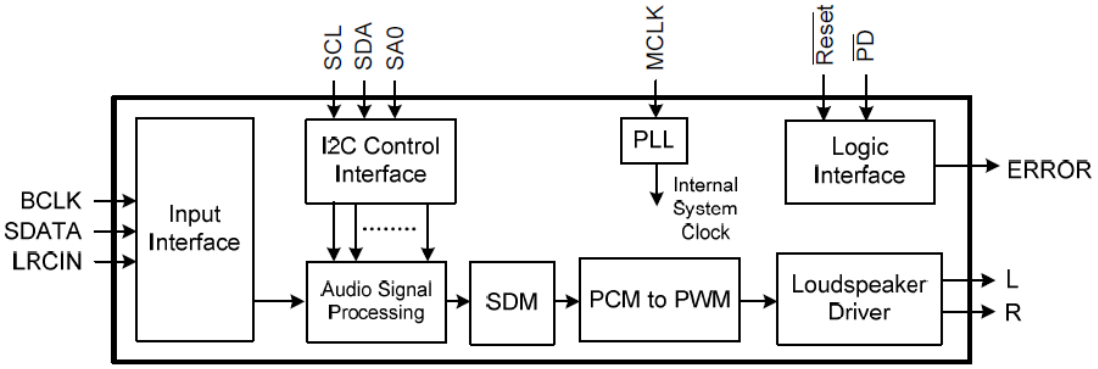


Figure 7 Functional Block Diagram

Symbol	Parameter	Min	Max	Units
VDDL/R	Supply for Driver Stage	-0.3	30	V
DVDD	Supply for Digital Circuit	-0.3	3.6	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

Table 6 : Absolute Maximum Ratings

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~26	V
T_A	Ambient Operating Temperature	0~70	°C

Table 7 Recommended Operating Conditions

C. HEADPHONE AMPLIFIER (U5)

Description

The AD22657B is a 2-Vrms cap-less stereo line driver. The device is ideal for single supply electronics. Cap-less design can eliminate output dc-blocking capacitors for better low frequency response and save cost.

The AD22657B is capable of delivering 2-Vrms output into a 10k ohm load with 3.3V supply. The gain settings can be set by users from 1V/V to 10V/V externally. The AD22657B has under voltage protection to prevent POP noise. Build-in shutdown control and de-pop control sequence also help AD22657B to be a pop-less device.

The AD22657B is available in a 10-pin MSOP package.

Features

- Operation Voltage: 3V to 3.6V
- Cap-less Output
    - Eliminates Output Capacitors
    - Improves Low Frequency Response
    - Reduces POP/Clicks
- Low Noise and THD
    - Typical SNR 107dB
    - Typical Vn 7uVrms
    - Typical THD+N < 0.02%
- Maximum Output Voltage Swing into 2.5k Load
    - 2Vrms at 3.3V Supply Voltage
- Single-ended Input
- External Gain Setting from 1V/V to 10V/V
- Fast Start-up Time: 0.5ms
- Integrated De-Pop Control
- External Under Voltage Protection
- Thermal Protection
- Less External Components Required
- +/-8kV IEC ESD Protection at line outputs

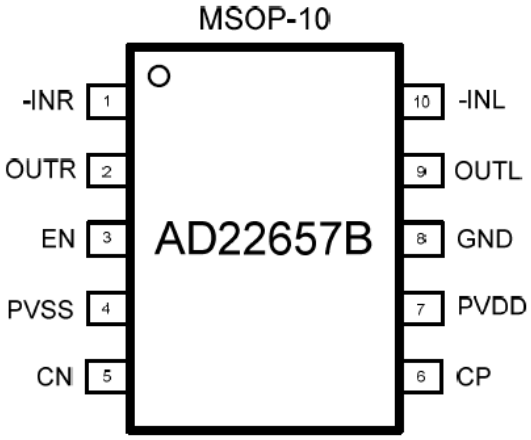


Figure 8 Pin description

No.	Name	Type (1)	Pin Description
1	-INR	I	Right channel OP negative input
2	OUTR	O	Right channel OP output
3	EN	I	Enable input, active high
4	PVSS	P	Supply voltage
5	CN	I/O	Charge-pump flying capacitor negative terminal
6	CP	I/O	Charge-pump flying capacitor positive terminal
7	PVDD	P	Positive supply
8	GND	P	Ground
9	OUTL	O	Left channel OP output
10	-INL	I	Left channel OP negative input

Table 8 Pin functions

SYMBOL	PARAMETER		Min	NOM	Max	UNIT
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IH}	High Level Input Voltage	EN		60		% of V_{DD}
V_{IL}	Low Level Input Voltage	EN		40		% of V_{DD}
T_A	Operating Ambient Temperature Range		-40		85	℃
R_L	Load Resistance		600			Ω

Table 9 Recommended operating conditions

5. POWER STAGE

Power socket is used for taking voltages which are 12V_stby and 24V (VDD_Audio for 10W option via power_pin1). These voltages are produced in power card. Also socket is used for giving dimming, backlight and stand-by signals with power card. It is shown in figure.

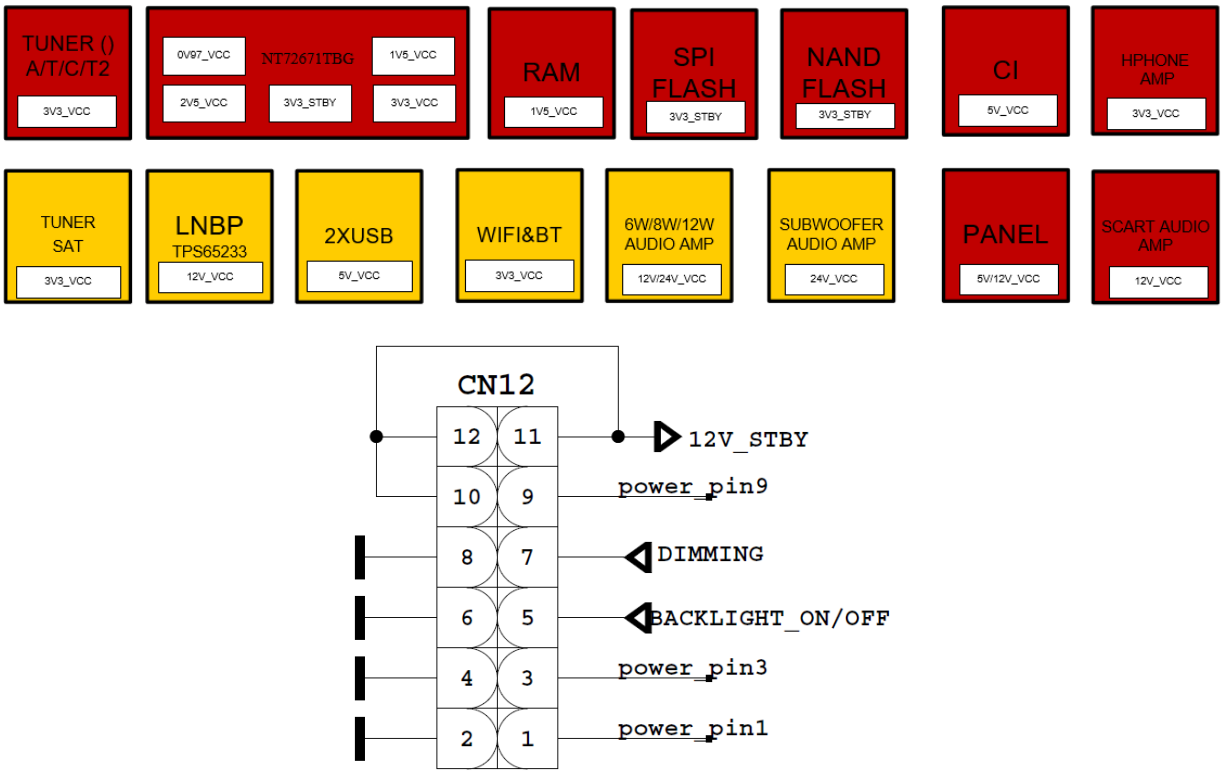


Figure 9 Power socket and power options

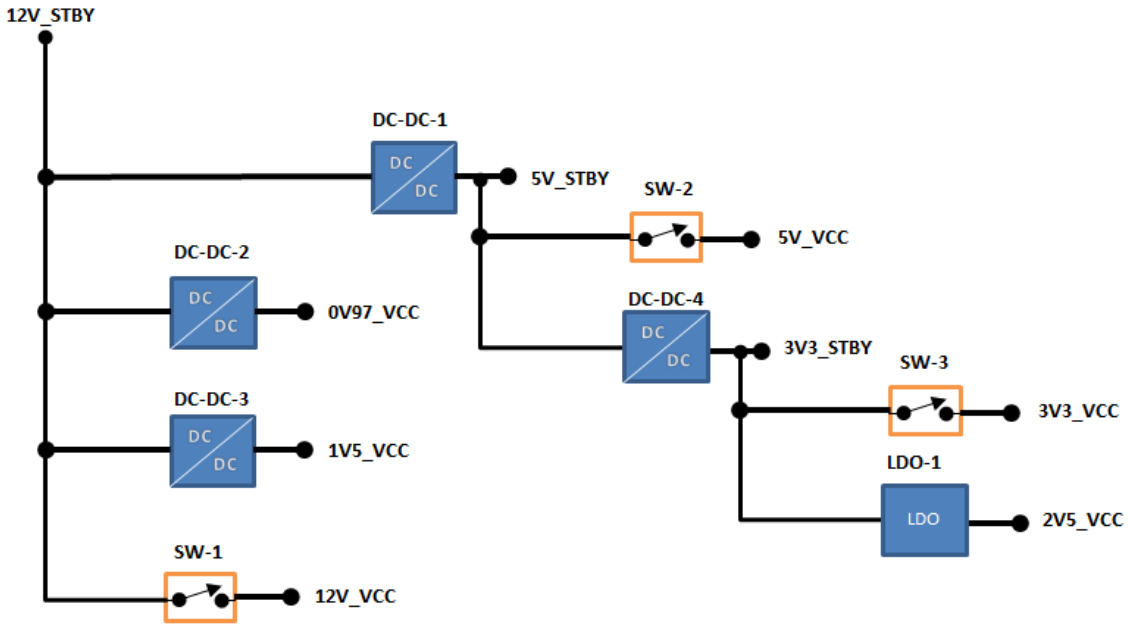


Figure 10 Power Distrubution

List of the components are:

- SW1(Q61-Q2) → UPA1919TE
- SW2(Q77) → DMG6402LDM
- DC-DC1 (U63) → TPS54528
- DC-DC2(U4) → TPS54528
- DC-DC3 (U128) → MP1470HGJ
- DC-DC4 (U10) → MP8774GQ-Z
- LDO1(U143) → APL5910

A. UPA1919TE

Description and Features

DESCRIPTION

The μPA1919 is a switching device, which can be driven directly by a 2.5 V power source.

This device features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

FEATURES

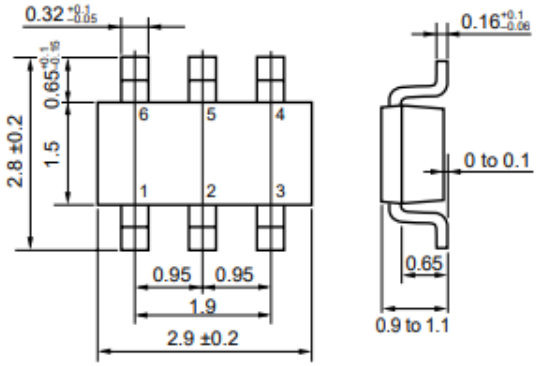
- 2.5 V drive available
- Low on-state resistance
  $R_{DS(on)1}$ = 58 mΩ MAX. (V_{GS} = –4.5 V, I_D = –3.0 A)
  $R_{DS(on)2}$ = 60 mΩ MAX. (V_{GS} = –4.0 V, I_D = –3.0 A)
  $R_{DS(on)3}$ = 84 mΩ MAX. (V_{GS} = –2.5 V, I_D = –3.0 A)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1919TE	SC-95 (Mini Mold Thin Type)

Marking: TX

PACKAGE DRAWING (Unit: mm)



1, 2, 5, 6 : Drain
3 : Gate
4 : Source

B. DMG6402LDM

Features

- Low RDS(ON)
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Lead Free By Design/RoHS Compliant (Note 1)
- Qualified to AEC-Q101 Standards for High Reliability

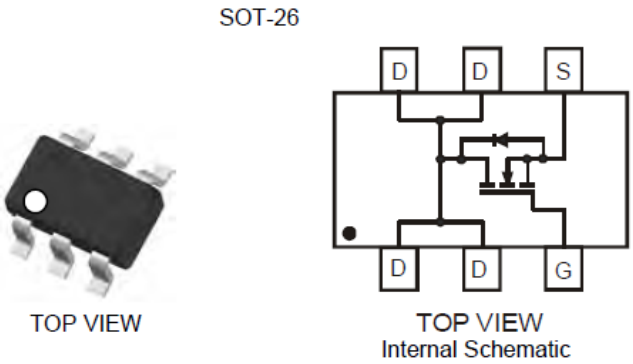


Figure 11 Pin description

C. TPS54528

Description

The TPS54528 is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54528 enables system designers to complete the suite of various end-equipment power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54528 uses the D-CAP2™ mode control that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Eco-mode™ operation at light loads. Eco-mode™ allows the TPS54528 to maintain high efficiency during lighter load conditions. The TPS54528 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V VIN input. The output voltage can be programmed between 0.76 V and 6.0 V. The device also features an adjustable soft start time. The TPS54528 is available in the 8-pin DDA package, and designed to operate from –40 C to 85 C.

Features

- D-CAP2™ Mode Enables Fast Transient Response
- Low Output Ripple and Allows Ceramic Output Capacitor
- Wide VIN Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.76 V to 6.0 V
- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications
    - 65 mΩ (High Side) and 36 mΩ (Low Side)
- High Efficiency, less than 10 μA at shutdown
- High Initial Bandgap Reference Accuracy
- Adjustable Soft Start
- Pre-Biased Soft Start
- 650-kHz Switching Frequency (fSW)

- Cycle By Cycle Over Current Limit
- Auto-Skip Eco-mode™ for High Efficiency at Light Load

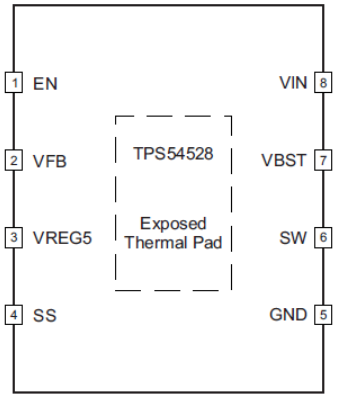


Figure 12 Pin Description

PIN		DESCRIPTION
NAME	NO.	
EN	1	Enable input control. EN is active high and must be pulled up to enable the device.
VFB	2	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	5.5 V power supply output. A capacitor (typical 1 µF) should be connected to GND. VREG5 is not active when EN is low.
SS	4	Soft-start control. An external capacitor should be connected to GND.
GND	5	Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.
SW	6	Switch node connection between high-side NFET and low-side NFET.
VBST	7	Supply input for the high-side FET gate drive circuit. Connect 0.1µF capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.
VIN	8	Input voltage supply pin.
Exposed Thermal Pad	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.

Table 10 Pin Functions

D. MP1470HGJ

Description

The MP1470 is a high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a very compact solution to achieve a 2A continuous output current over a wide input supply range, with excellent load and line regulation. The MP1470 has synchronous-mode operation for higher efficiency over the output current-load range. Current-mode operation provides fast transient response and eases loop stabilization. Protection features include over-current protection and thermal shutdown. The MP1470 requires a minimal number of readily-available, standard, external components and is available in a space-saving 6-pin TSOT23 package.

Features

• Wide 4.7V-to-16V Operating Input Range

• 163mΩ/86mΩ Low-RDS(ON) Internal Power MOSFETs

• Proprietary Switching-Loss–Reduction Technique

• High-Efficiency Synchronous-Mode Operation

• Fixed 500kHz Switching Frequency

• Internal AAM Power-Save Mode for High Efficiency at Light Load

• Internal Soft-Start

• Over-Current Protection and Hiccup

• Thermal Shutdown

• Output Adjustable from 0.8V

• Available in a 6-pin TSOT-23 package

PACKAGE REFERENCE

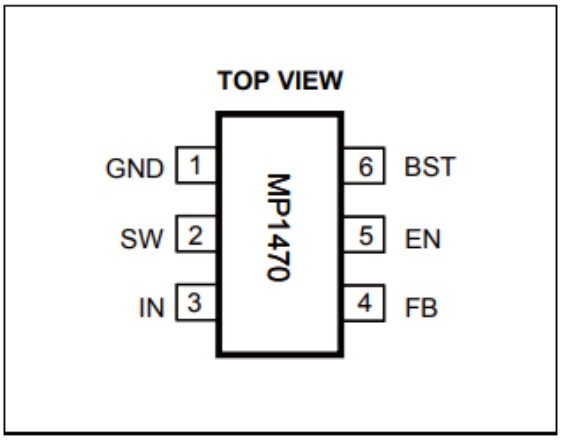


Figure 13 Pin Description

PIN FUNCTIONS

Package Pin #	Name	Description
1	GND	System Ground. Reference ground of the regulated output voltage: requires extra care during PCB layout. Connect to GND with copper traces and vias.
2	SW	Switch Output. Connect using a wide PCB trace.
3	IN	Supply Voltage. The MP1470 operates from a 4.7V-to-16V input rail. Requires C1 to decouple the input rail. Connect using a wide PCB trace.
4	FB	Feedback. Connect to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency fold-back comparator lowers the oscillator frequency when the FB voltage drops below 140mV to prevent current-limit runaway during a short circuit fault.
5	EN	EN=HIGH to enable the MP1470. For automatic start-up, connect EN to V_{IN} using a 100kΩ resistor.
6	BST	Bootstrap. Connect a capacitor and a resistor between SW and BS pins to form a floating supply across the high-side switch driver. Use a 1μF BST capacitor.

Table 11 Pin Functions

E. MP8774GQ-Z

Description

The MP8774 is a fully integrated high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. The MP8874 offers a very compact solution that achieves 12A of continuous output current with excellent load and line regulation over a wide input range. The MP8774 uses synchronous mode operation for higher efficiency over the output current load range. Constant-on-time (COT) control operation provides very fast transient response, easy loop design, and very tight output regulation. Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown. The MP8774 requires a minimal number of readily available, standard, external components and is available in a space-saving QFN-16 (3mmx3mm) package.

Features

- Output Adjustable from 0.6V
- Wide 3V to 18V Operating Input Range
- 12A Output Current
- 16mΩ/5.5mΩ Low RDS(ON) Internal Power MOSFETs
- 100μA Quiescent Current
- High-Efficiency Synchronous Mode Operation
- Pre-Biased Start-Up
- Fixed 700kHz Switching Frequency
- External Programmable Soft Start-Up Time
- Enable (EN) and Power Good (PG) for Power Sequencing
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Available in a QFN-16 (3mmx3mm) Package

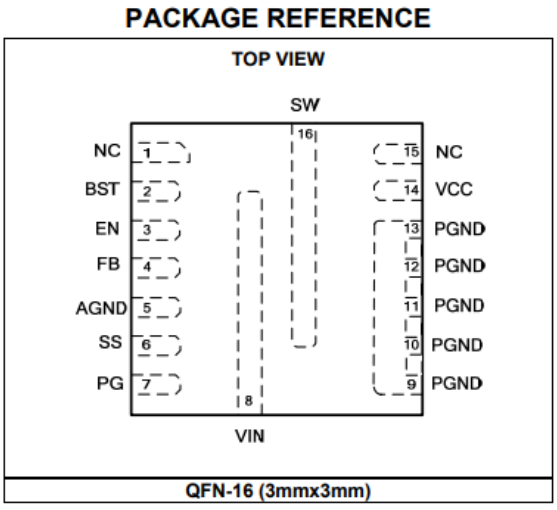


Figure 14 Pin Descriptions

PIN FUNCTIONS

Package Pin #	Name	Description
1, 15	NC	**No connection.** NC must be left floating.
2	BST	**Bootstrap.** Connect a capacitor between SW and BST to form a floating supply across the high-side switch driver. A BST resistor less than 4.7Ω is recommended.
3	EN	**Enable.** Pull EN high to enable the MP8774. When floating, EN is pulled down to GND and disabled by an internal 1.2MΩ resistor.
4	FB	**Feedback.** FB sets the output voltage when connected to the tap of an external resistor divider between output and GND.
5	AGND	**Signal ground.** AGND is not connected to the system ground internally. Ensure that AGND is connected to the system ground in the PCB layout.
6	SS	**Soft start.** Connect a capacitor across SS and GND to set the soft-start time to avoid inrush current at start-up.
7	PG	**Power good output.** The output of PG is an open drain. PG changes state if UVP, OCP, OTP, or OV occurs.
8	VIN	**Supply voltage.** The MP8774 operates from a 3 - 18V input rail. A capacitor (C1) is needed to decouple the input rail. Use a wide PCB trace to make the connection.
9 - 13	PGND	**System ground.** PGND is the reference ground of the regulated output voltage. PGND requires careful consideration during the PCB layout. PGND is recommended to be connected to GND with coppers and vias.
14	VCC	**Internal bias supply output.** Decouple VCC with a 1μF capacitor. Place the VCC capacitor close to VCC and GND.
16	SW	**Switch output.** Connect SW with a wide PCB trace.

Table 12 Pin Functions

F. APL5910

Description

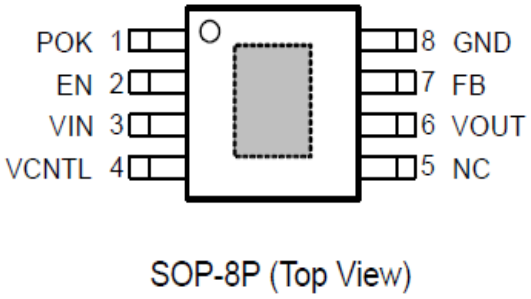
The APL5910 is a 1A ultra low dropout linear regulator. The IC needs two supply voltages, one is a control voltage (VCNTL) for the control circuitry, the other is a main supply voltage (VIN) for power conversion, to reduce power dissipation and provide extremely low dropout voltage. The APL5910 integrates many functions. A Power-On- Reset (POR) circuit monitors both supply voltages on VCNTL and VIN pins to prevent erroneous operations. The functions of thermal shutdown and current-limit protect the device against thermal and current over-loads. A POK indicates that the output voltage status with a delay time set internally. It can control other converter for power sequence. The APL5910 can be enabled by other power systems. Pulling and holding the EN voltage below 0.4V shuts off the output.

The APL5910 is available in a SOP-8P package which features small size as SOP-8 and an Exposed Pad to reduce the junction-to-case resistance to extend power range of applications.

Features

- Ultra Low Dropout
    - 0.12V (Typical) at 1AOutput Current
- 0.8V Reference Voltage
- High Output Accuracy
    - ±1.5%over Line, Load, and Temperature Range
- Fast Transient Response

- Adjustable Output Voltage
- Power-On-Reset Monitoring on Both VCNTL and VIN Pins
- Internal Soft-Start
- Current-Limit and ShortCurrent-Limit Protections
- Thermal Shutdown with Hysteresis
- Open-Drain VOUT Voltage Indicator (POK)
- Low Shutdown Quiescent Current (< 30mA)
- Shutdown/Enable Control Function
- Simple SOP-8P Package with Exposed Pad
- Lead Free and Green Devices Available (RoHS Compliant)



SOP-8P (Top View)

Figure 15 Pin Description

PIN		FUNCTION
NO.	NAME	
1	POK	Power-OK signal output pin. This pin is an open-drain output used to indicate the status of output voltage by sensing FB voltage. This pin is pulled low when output voltage is not within the Power-OK voltage window.
2	EN	Active-high enable control pin. Applying and holding the voltage on this pin below the enable voltage threshold shuts down the output. When re-enabled, the IC undergoes a new soft-start process. When left this pin open, an internal pull-up current (5μA typical) pulls the EN voltage and enables the regulator.
3	VIN	Main supply input pin for voltage conversions. A decoupling capacitor (≥10μF recommended) is usually connected near this pin to filter the voltage noise and improve transient response. The voltage on this pin is monitored for Power-On-Reset purpose
4	VCNTL	Bias voltage input pin for internal control circuitry. Connect this pin to a voltage source (+5V recommended). A decoupling capacitor (1μF typical) is usually connected near this pin to filter the voltage noise. The voltage at this pin is monitored for Power-On-Reset purpose.
5	NC	No Connection.
6	VOUT	Output pin of the regulator. Connecting this pin to load and output capacitors (10μF at least) is required for stability and improving transient response. The output voltage is programmed by the resistor-divider connected to FB pin. The VOUT can provide 1A (max.) load current to loads. During shutdown, the output voltage is quickly discharged by an internal pull-low MOSFET.
7	FB	Voltage Feedback Pin. Connecting this pin to an external resistor divider receives the feedback voltage of the regulator.

Table 13 Pin Functions

6. MICROCONTROLLER

NOVATEK NT72671TBG

Description

NT72671TBG is an integrated digital TV system-on-chip which complaints with variety ATV standards (NTSC, PAL and SECAM), and DTV standards (ISDB-T, DVB-T/-T2/-C/-S/-S2/-S2X, ITU-TJ.83B, 8VSB, and DTMB), and integrates DTV and multi-media AV decoder, SIF demodulator, and support A/V post-processing. The integrated video ADC and video decoder support PC VGA port, YPbPr or SCART, CVBS and SCART S-Video Input. The video decoder supports universal TV video format. The integrated audio ADC supports stereo audio input corresponding to video input sources. The integrated TV sound decoder supports universal TV sound format. The advanced picture quality and color engine create more vivid image impression than ever. The HDMI receiver v2.0 supports deep color, CEC features and 3D input formats. The USB high speed host supports updating firmware code, multi-media playback from the external USB flash devices.

The standby controller can operate solely from the main system, powered by the standby powersource from power module, consumes as low current as possible. It meets the requirement of Green appliance.

Features

- CPU
  - ARM Multi-cores
  - Support TrustZone
  - Support PTM
  - Support NEON
- DRAM Interface
  - MCM DDR3 1.866GHz 32bits 1GB
  - External DDR3 1.866GHz 32bits up to 1GB
  - Spread Spectrum PLL for EMI reduction
- Flash controller
  - eMMC 5.0 with HS400 type flash up to 180MHz clock rate
  - SPI NOR type flash x2
- Stand-by Controller
  - Support VGA / IR / KeyPad / CEC/ wake-up
  - Built-in Turbo 8051 for stand-by application usage
  - Built-in Low Voltage Reset for brown out
  - Built-in EDID for saving system BOM cost
  - System power control
- Condition Access
  - Support Common Interface
  - Support Common Interface Plus
  - Built-in Cryptograph Engine for conditional access and CI Plus
  - Meet Common Interface Plus's Robust and Compliance rule
- Copy Protection Engine
  - Support Cryptograph Key Protection
  - Support Demux Key Protection
  - Support HDCP Key Protection
- Internal High-Speed Video ADC
  - Integrated triple high speed ADCs/ PLL to support both YPbPr and RGB format signal
  - 10-bits data resolution
  - Maximum conversion up to 165 MSPS
  - Support 0.7 Volts analog RGB/YUV input
  - 3:1 analog input MUX
  - Supports both non-interlaced and interlaced input signals
- Analog Video Decoder
  - Clamp and AGC (Automatic Gain Control) circuit to support 0.5 to 1.6V analog input signal
  - Support multi-standards, macro-vision detection and related status report
  - Embedded Teletext Level 2.5 / Close Caption and other VBI Decoder
  - 2D and 3D adaptive Comb Filter for better Y/C Separation
  - Support VPS signal decode for EU channel sorting purpose
- TV encoder with built-in video DAC
  - Built-in 10-bit DAC for CVBS Analog Video output.
  - Support TTX/ CC/ WSS/ VPS/ CGMS-A/ Macrovision insertion
- Digital Video CODEC
  - Built-in multi-standard video codec
  - Support pixel format YUV420 only for all video codec except JPEG
  - H.264 Constrained Baseline/Main/High Profiles up to 3840x2160p30 (Level 5.0 and Level 5.1 under limited bit-rate)
  - VP8 Profiles @ 1080p60
  - VP9 Profile 0, 2 up to 10-bit @ 3840x2160p60
  - AVS(Optional) Jizhun Profile @ 1080p60 (Level 6.0)
  - AVS+(Optional) @ 1080p60
  - AVS2(Optional) @ 3840x2160p60
  - VC-1(Optional) Simple/Main/Advanced Profiles @ 1080p60 (Level 3.0)
  - RealVideo(Optional) 8/9/10 @ 1080p60
  - MPEG-4 Simple/Advanced Simple Profiles @ 1080p60
  - H.263 Profile 0 @ 1080p60
  - DivX 3.11/4/5/6(Optional) @ 1080p60
  - Sorenson Spark @ 1080p60
  - MPEG-2 Main Profile @ 1080p60
  - MPEG-1 @ 1080p60
  - JPEG baseline sequential mode
    - Support pixel formats in YUV420, YUV422 and YUV444
    - Support Motion JPEG @ 1080p60
  - HEVC(H.265) Main 10 profile @

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3840x2160p60 (level 5.1)
- SHVC (ATSC 3.0) base layer up to Main 10 @ 1080p60 (level 4.1) + enhance layer up to Main 10 3840x2160p60 (level 5.1)
- H.264 encoder @ 1080p30, @720p60, @480p60
- JPEG encoder baseline YUV420 @ 1080p10
- Support video rotation function
  - YUV420: up to UHD 30fps, 10-bit
  - YUV422/ YUV444: up to FHD 60fps, 8-bit

■ De-Interlacing
- 5th generation High performance Motion-Adaptive De-interlacing
- 5th generation Diagonal Edge Enhancement for smoothing edge outline
- Automatic Video Source Detection
- Support Inverse 3:2/2:2 pull down and multiple cadence for film stream
- Scene Change Detection
- Built-in Anti-Crosscolor to remove abnormal color performance
- Built-in Color Performance stabilizer for SECAM video format
- Built-in Region Classifier engine to get flicker free image quality

■ Visual Effect Processor
- 5th generation Advanced Scaling Up Engine
- Support Nonlinear Scaling
- 5th generation LTI/CTI function
- Support 5th Color Engine
- Global Brightness, Contrast, Hue Saturation and Intensity Adjustment
- Built-in I-Gamma and Black Stretch for Automatic Contrast Adjustment
- Support sRGB and xvYCC Adjustment Standard
- De-blocking, De-Mosquito, Temporal and Spatial Noise Filter
- Adaptively determine 3D noise filter for different noise level
- SQUARE (Sparse Qualified Artifact Removing Engine): a Best-in-Class Noises & Artifacts Reducer.
- SD2HD detection and Processing
- DP Meter for Dynamic backlight Control
- Support Cinema Contrast Enhancer
- Bipp (Bit Depth Plus): bit-depth increasing and smoothing false contours
- 3DLUT for Gamut Mapping
- Support HDR (HDR10, HLG)
- Support Dynamic HDR

■ Display Processor
- Support 8 Lane Vby1 for UHD60P Video
- Embedded dual 10-bit LVDS transmitter
- Supports single pixel / dual pixel output
- Dithering function supports 30-bit quality for 24 bit or 18-bit panel
- Optional Frame Sync or Free Run display synchronization modes
- Display Resolution up to 3840X2160@60Hz UHD TV format
- Support UHD MEMC
- Support Watermark processor
- Built-in Gamma Correction for different type display device
- Supports Pivot (H flipping display)
- V flipping is in LBM
- Support H/V sync out
- Video alpha blending
- Support Local Dimming Control

■ 3D-Graphic Engine
- Mali Multi-cores
- OpenGL® ES 1.1, 2.0

■ 2D-Graphic Engine
- Bitmap Operation
- ARGB/RGBA format
- Copy/Color expansion
- Logic Operation
- Copy with alpha blending (only 16/32 bit color mode)
- Source and destination area could be overlapped
- Color key for the transparence effect
- 12 Raster Operation (ROP) rules
- Fill Rectangle
- Color fill
- Gradient fill
- Scaling
- Bicubic Algorithm

■ OSD
- 8/16/32-bit OSD Architecture
- 3 OSD Layers
- 7 levels of transparency with pixel or frame based operation (background, video, Plane3, Plane2, Plane1, cursor1,

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cursor2)
- Support OSD H/V scaling up/down function
- Programmable width & height to meet LCD/TV's resolution exactly

■ HDMI receiver
- 4 HDMI 2.0 Input ports
- Support 4K2K 60P input
- Support HDMI PIP
- HDMI Rx 1.4b Compliant
- Integrated HDCP 1.4 & 2.2 cipher engine for Content Protection
- Support High-Level CEC Command for Easy Link between CE equipments.
- Support Deep Color for more pixel depth information
- Support xvYCC for wide color gamut application
- Support 3D input
- Support fast switching function
- Support Audio 2~8 channel 32-192KHz
- Support ARC (Audio Return Channel)

■ Digital VIF Demodulator
- Compliant with NTSC, PAL, SECAM video standards for universal analog terrestrial and cable support
- Support for FM-A2(IRT-A2), AM, BTSC+SAP, MK-A2, NICAM audio standards
- Support Low IF, 5 ~ 8 MHz (silicon tuner)
- Single IF AGC control with ΔΣ modulation
- Flexible channel bandwidth (6 MHz, 7 MHz, and 8 MHz)
- Digital video and audio dual-path split processor

■ SIF Demodulator
- NICAM-BG/DK/I/L, A2-BG/DK/I, BTSC, A2-M, AM SECAM-L
- Automatic standard and mode detection
- Automatic carrier mute and automatic NICAM fall back
- 32KHz audio output

■ Audio CODEC (Audio ADC/DAC)
- Built-in 3:1 audio ADC input mux (MAX. sampling rate 48 KHz)
- Built-in 2 audio DAC output (MAX. sampling rate 48 KHz)
- Built-in 2 I2S Output format for Power-Stage Amplifier
- Built-in 1 I2S Input
- S/PDIF output supported

■ Audio Processor
- Dedicated dual DSP to decode compressed audio and post-processing
- Supports digital audio format decoding:
  - MPEG-1/2 (Layer I/ II/ III), Dolby Digital (AC3) (Optional), Dolby Digital Plus (EAC3) (Optional), AC4 (Optional), AAC-LC (Optional) HE-AAC (Optional), WMA3 (Optional), WMA (Optional), DTS (Optional), MPEG-H (Optional), OPUS
- Supports Dolby Digital Plus (Optional) and MS10/11/12 (Optional) multistream decoder, including Dolby Digital Encoder for transcoding streams to Dolby Digital 5.1
- Support DTS M6 (Optional)
- Supports DTS Neo 2:5 (Optional) to transcoding streams to DTS 5.1
- Advance sound processing: Automatic Volume Control, 5-band EQ, Automatic Gain Control, Virtual Surround, Dynamic range control (DRC)
- Advance sound processing options available, for example: DTS Trusurround HD (Optional), DTS Studio Sound (Optional)

■ ISDB-T Demodulator
- Compliance with ISDB-T standard ARIB STD-B31 and SBTVD standard ABNT NBR 15601
- Receiver specifications ARIB STD-B21 and ABNT NBR 15604 fulfilled
- Channel bandwidth 6, 7 and 8 MHz supported
- Low IF with configurable mixing frequency
- Single IF AGC control with ΔΣ modulation
- Partial (1-segment) and full (13-segment) reception supported
- Non-hierarchical (single-layer) & hierarchical (layers A/B/C) reception supported
- Automatic detection of transmission parameters:
  - Mode: 1 (2k), 2 (4k), 3 (8k)
  - Guard interval ratio: 1/4, 1/8, 1/16, 1/32
  - Constellation: DQPSK, QPSK, 16QAM, 64QAM

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- Code rate: 1/2, 2/3, 3/4, 5/6, 7/8
- Wake-up flag for emergency warning broadcasting application
- Automatic spectral inversion
- Robust TMCC decoding
- Impulsive noise reduction
- Adjacent-channel interference suppression
- Superior AWGN and multipath performance
- Superior co-channel interference performance
- Timing acquisition range: ±100 ppm
- Carrier acquisition range: ±400 kHz (6 MHz bandwidth)

■ DVB-T Demodulator
- Compliance with DVB-T standard ETSI EN 300 744
- Receiver specifications NorDig Unified 2.5, D-Book 7, and Digitenne 4.0.4 fulfilled
- Channel bandwidth 6, 7 and 8 MHz supported
- Low IF with configurable mixing frequency
- Single IF AGC control with ΔΣ modulation
- Non-hierarchical and hierarchical (HP/LP) reception supported
- Automatic detection of transmission parameters:
  - Mode: 2K, 8K
  - Guard interval ratio: 1/4, 1/8, 1/16, 1/32
  - Constellation: QPSK, 16QAM, 64QAM
  - Code rate: 1/2, 2/3, 3/4, 5/6, 7/8
- Automatic spectral inversion
- Robust TPS decoding
- Impulsive noise reduction
- Superior co-channel interference performance
- Superior AWGN and multipath performance
- Timing acquisition range: ±100 ppm
- Carrier acquisition range: ±650 kHz (8 MHz bandwidth)

■ DVB-C Demodulator
- Compliance with DVB-C standard ETSI EN 300 429
- Receiver specifications NorDig Unified 2.2.2, Ziggo and China HD_GY/T 241-2009 fulfilled
- Variable symbol rate 1 ~ 7.2 Mbaud supported
- Low IF with configurable mixing frequency
- Single IF AGC control with ΔΣ modulation
- Constellations 16QAM, 32QAM, 64QAM, 128QAM and 256QAM
- Roll-off factor 0.15
- Robust blind adaptive equalizer
- Superior impulsive noise cancellation

■ ATSC Demodulator
- Compliance with ATSC 8VSB standard A/53 Annex D
- Channel bandwidth 6 MHz supported
- Low IF supported with configurable mixing frequency
- Single IF AGC control with ΔΣ modulation
- Excellent ATSC 50-channel and Brazil A/B/C/D/E reception performance
- Excellent phase noise tracking performance
- Excellent co-channel interference performance
- Timing acquisition range: ±100 ppm
- Carrier acquisition range: ±200 kHz

■ J.83B Demodulator
- Compliance with digital television cable system standard ITU-T J.83 Annex B
- Channel bandwidth 6 MHz supported
- Low IF supported with configurable mixing frequency
- Single IF AGC control with ΔΣ modulation
- Automatic detection of 64/256QAM
- Robust blind adaptive equalization
- Superior impulsive noise cancellation
- Excellent phase noise tracking performance
- Excellent co-channel single-tone rejection capability
- Timing acquisition range: ±100 ppm
- Carrier acquisition range: ±400 kHz (64QAM)

■ DVB-T2
- Compliance with DVB-T2 standard ETSI EN 302 755
- Receiver specifications NorDig-Unified 2.5 and D-Book 7 fulfilled
- Channel bandwidth 1.7, 5, 6, 7, and 8 MHz supported
- Low IF supported with configurable mixing

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frequency
- All single-profile modes supported, including
  - T2-Base profile
  - T2-Lite profile
  - Single and multiple PLPs
  - SISO and MISO transmissions
  - Rotated and non-rotated constellations
  - Scrambled L1-post signaling
- Automatic spectral inversion
- Robust L1 decoding
- Superior multipath performance
- Excellent co-channel interference suppression
- Fast channel zapping
- Timing acquisition range: ±100 ppm
- Carrier acquisition range: ±650 kHz (8 MHz bandwidth)

■ DVB-S/S2/S2X
- Compliant with broadcast service configurations of DVB-S standard ETSI EN 300 421, DVB-S2 standard EN 302 307-1, and DVB-S2X standard EN 302 307-2
- Symbol Rate 1 ~ 45 Msps for QPSK/8PSK/8APSK, 1 ~ 39 Msps for 16APSK, and 1 ~ 32 Msps for 32APSK
- Roll-off factors from 0.05 to 0.35
- Constellations QPSK, 8PSK, 8APSK, 16APSK and 32APSK
- Dual ADC interface with differential and single-ended IQ input
- IQ imbalance compensation
- Automatic spectrum inversion
- Fast blind scan
- Compliance with DiSEqC™ v2.2

■ DTMB
- Compliance with DTMB standard GB 20600-2006
- Receiver specifications GB/T 26683 and GB/T 26686 fulfilled
- Channel bandwidth 6, 7 and 8 MHz supported
- Automatic working mode detection
- Carrier number: 1, 3780
- Guard interval length: 420, 595, 945
- Constellation: 4QAM, 4QAM-NR, 16QAM, 32QAM, 64QAM
- Code rate: 0.4/0.6/0.8
- Large carrier acquisition range
- Superior AWGN and multipath performance

■ Ethernet
- Built-in 10/100 Ethernet MAC and PHY
- Support WOL

■ USB host/device controller with built in transceiver
- 1 USB 3.0 host port
- 3 USB 2.0 host ports
- Compliant with USB Specification Revision 2.0
- Support high-speed, full-speed and low-speed devices
- Integrated USB 2.0 transceiver

■ LED backlight
- PWM x 2
- PWM delay and duty is adjustable individually
- PWM delay is phase-locked to VS
- Support PWM frequency = 1 x VS , 2 x VS frequency
- SPI LED-driver interface

■ Tcon function
- P2P TX support USIT, CEDS/EPI, ISP/CSPI, BOE
- Support OD
- Support RGBW 2.0
- Support Dual gamma
- Support Demura function

■ Miscellaneous
- Support ATSC3.0 Link-Layer Protocol input interface, Built-in UART controller

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD}	0.97V power supply	0.9215	0.97	1.0185	V	
$V_{1.5V}$	1.5V power supply (DDR3)	1.425	1.5	1.575	V	
$V_{1.8V}$	1.8V power supply (eMMC)	1.7	1.8	1.9	V	
$V_{2.5V}$	2.5V power supply	2.375	2.5	2.625	V	
V_{DDIO}	3.3V power supply	3.135	3.3	3.465	V	
V_{IN3}	3.3V I/O with 5V Tolerance	0	3.3	5.25	V	
	Input voltage of 3.3V I/O	0	3.3	3.465	V	

Table 14 Recommended Operating Conditions

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7. 2GB DDR3 SDRAM

NANYA NT5CB128M16JR-FL 2133 (U3)

Description

The 2Gb Double-Data-Rate-3 (DDR3(L)) is double data rate architecture to achieve high-speed operation. It is internally configured as an eight bank DRAMs.

The 2Gb chip is organized as 32Mbit x 8 I/Os x 8 banks or 16Mbit x 16 I/Os x 8 bank devices. These synchronous devices achieve high speed double-data-rate transfer rates of up to 1866 Mb/sec/pin for general applications.

The chip is designed to comply with all key DDR3(L) DRAM key features and all of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CK rising and $\overline{CK}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS pair in a source synchronous fashion.

These devices operate with a single 1.5V ± 0.075V or 1.35V -0.067V/+0.1V power supply and are available in BGA packages.

Features

- **JEDEC DDR3 Compliant**
  - 8n Prefetch Architecture
  - Differential Clock(CK/$\overline{CK}$) and Data Strobe(DQS/$\overline{DQS}$)
  - Double-data rate on DQs, DQS and DM
- **Data Integrity**
  - Auto Self Refresh (ASR) by DRAM built-in TS
  - Auto Refresh and Self Refresh Modes
- **Power Saving Mode**
  - Partial Array Self Refresh (PASR)[1]
  - Power Down Mode
- **Signal Integrity**
  - Configurable DS for system compatibility
  - Configurable On-Die Termination
  - ZQ Calibration for DS/ODT impedance accuracy via external ZQ pad (240 ohm ± 1%)
- **Signal Synchronization**
  - Write Leveling via MR settings [7]
  - Read Leveling via MPR
- **Interface and Power Supply**
  - SSTL_15 for DDR3:VDD/VDDQ=1.5V(±0.075V)
  - SSTL_135[4] for DDR3L:VDD/VDDQ=1.35V(-0.067/+0.1V)

Symbol	Parameter		Rating			Unit	Note
			Min.	Typ.	Max.		
VDD	Supply Voltage	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6
VDDQ	Supply Voltage for Output	DDR3	1.425	1.5	1.575	V	1,2
		DDR3L	1.283	1.35	1.45		3,4,5,6

Table 15 Recommended Operating Conditions

8. 4GBIT (256M X 8 BIT) NAND FLASH MEMORY

MT29F4G08ABAEAWP (U133)

Description

Micron NAND Flash devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (I/Ox) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection and monitor device status (R/B#). This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign. A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). There is at least one NAND Flash die per chip enable signal. For further details, see Device and Array Organization. This device has an internal 4-bit ECC that can be enabled using the GET/SET features or by factory (always enabled). See Internal ECC and Spare Area Mapping for ECC for more information.

Features

- Open NAND Flash Interface (ONFI) 1.0-compliant
- Single-level cell (SLC) technology
- Organization
    - Page size x8: 4320 bytes (4096 + 224 bytes)
    - Page size x16: 2160 words (2048 + 112 words)
    - Block size: 64 pages (256K + 14K bytes)
    - Plane size: 2 planes x 1024 blocks per plane
    - Device size: 4Gb: 2048 blocks
- Asynchronous I/O performance
    - ^{t}RC/^{t}WC: 20ns (3.3V), 30ns (1.8V)
- Array performance
    - Read page: 25µs
    - Program page: 200µs (TYP)
    - Erase block: 2ms (TYP)
- Command set: ONFI NAND Flash Protocol
- Advanced command set
    - Program page cache mode
    - Read page cache mode
    - One-time programmable (OTP) mode

    - Programmable drive strength
    - Two-plane commands
    - Multi-die (LUN) operations
    - Read unique ID
    - Block lock (1.8V only)
    - Internal data move
- Operation status byte provides software method for detecting
    - Operation completion
    - Pass/fail condition
    - Write-protect status
- Ready/Busy# (R/B#) signal provides a hardware method of detecting operation completion
- WP# signal: Write protect entire device
- First block (block address 00h) is valid when shipped from factory with ECC. For minimum required ECC, see Error Management.
- RESET (FFh) required as first command after power-on
- Alternate method of device initialization after power up (contact factory)
- Internal data move operations supported within the plane from which data is read
- Quality and reliability
    - Data retention: JESD47G-compliant; see qualification report
    - Endurance: See Qualification Report
- Operating voltage range
    - VCC: 2.7–3.6V
    - VCC: 1.7–1.95V
- Operating temperature:
    - Commercial: 0°C to +70°C
    - Industrial (IT): –40ºC to +85ºC
- Package
    - 48-pin TSOP type 1, CPL2
    - 63-ball VFBGA

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	–	70	°C
	Industrial		–40	–	85	°C
Vcc supply voltage	1.8V	V_{CC}	1.7	1.8	1.95	V
	3.3V		2.7	3.3	3.6	V
Ground supply voltage		V_{SS}	0	0	0	V

Table 16 Recommended Operating Conditions

9. 16M-BIT [16M X 1] CMOS SERIAL FLASH EEPROM

KH25L1606EM2-12G MACRONIX SPI FLASH (U135)

Description

The device features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input. When it is in Dual Output read mode, the SI and SO pins become SIO0 and SIO1 pins for data output. The device provides sequential read operation on whole chip. After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page basis, or word basis for erase command is executes on sector, or block, or whole chip basis. To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit. Advanced security features enhance the protection and security functions; please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode. The device utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after typical 100,000 programs and erase cycles.

Features

- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 16,777,216 x 1 bit structure or 8,388,608 x 2 bits (Dual Output mode) structure
- 512 Equal Sectors with 4K byte each
  - Any Sector can be erased individually
- 32 Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Program Capability
  - Byte base
  - Page base (256 bytes)
- Latch-up protected to 100mA from -1V to Vcc +1V

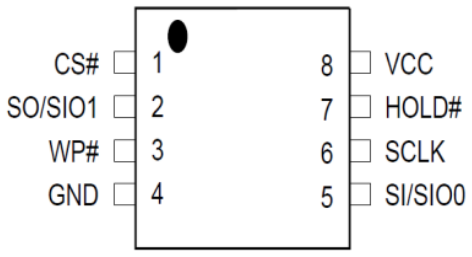


Figure 16 Pin configuration

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for Dual Output mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Output (for Dual Output mode)
SCLK	Clock Input
WP#	Write protection
HOLD#	Hold, to pause the device without deselecting the device
VCC	+ 3.3V Power Supply
GND	Ground

Table 17 Pin Description

10. USB INTERFACE

Novatek IC has four input ports for USB, and therefore it doesn't need any hub IC.

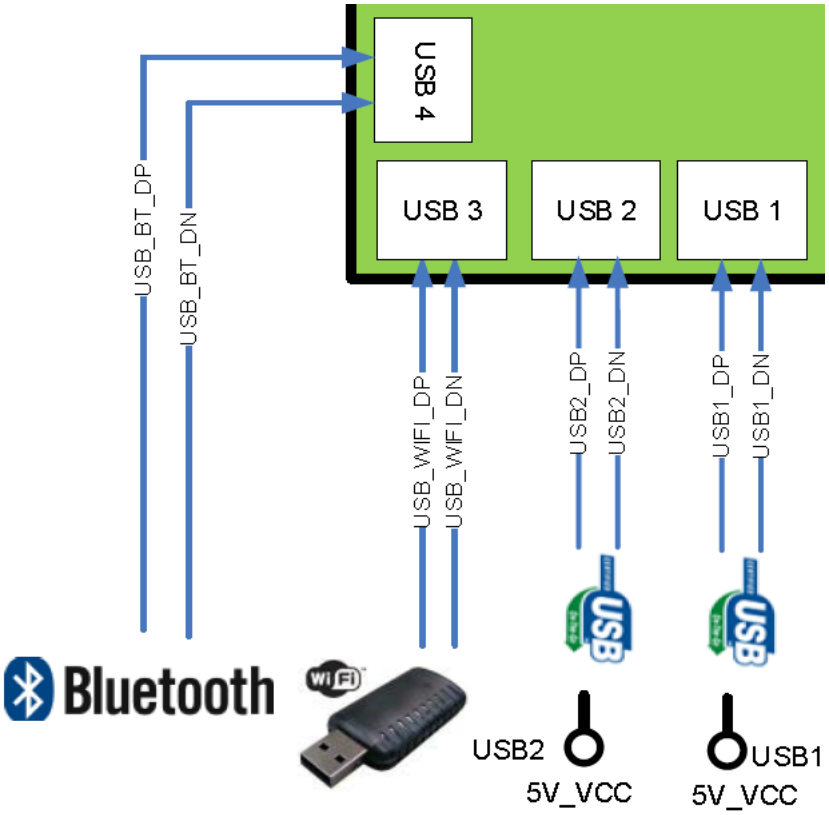


Figure 17 USB Block Diagram

11. CI INTERFACE

17MB230 Digital CI ve Smart Card Interface Block diagram:

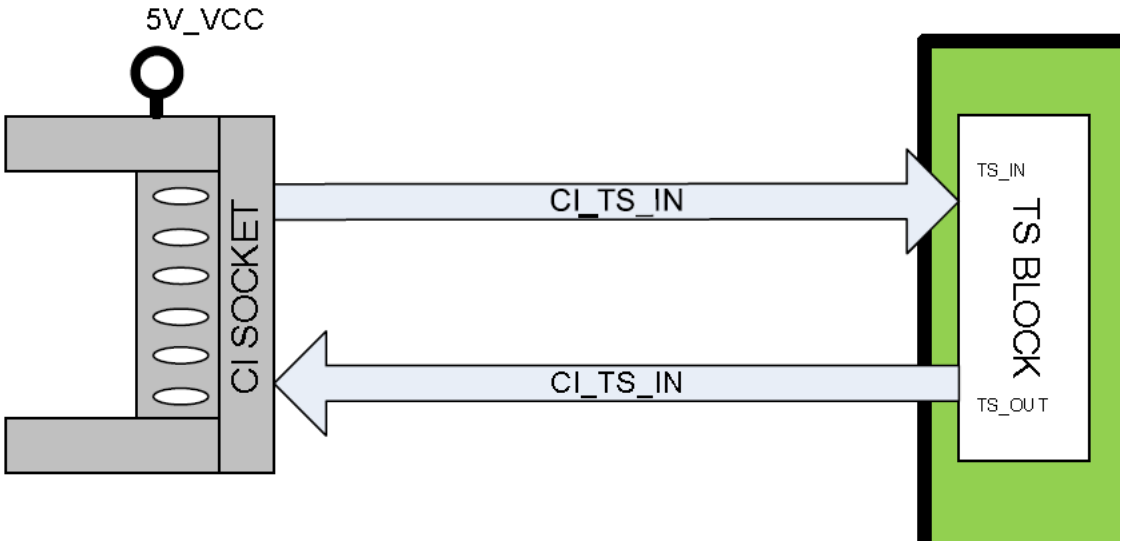


Figure 18 : CI interface

12. SOFTWARE UPDATE

MAIN SW UPDATE

In MB230 project, please follow software update procedure:

1. kylo_usb_update.bin, kylo_usb_update.scr, kylo_usb_update.scr.core and upgrade_mb230.bin files should be copied directly inside of a flash memory (not in a folder).
2. Insert flash memory to the TV when TV is powered off.
3. While pushing the OK button in remote control, power on and wait. TV will power-up itself.
4. If First Time Installation screen comes, it means software update procedure is successful.

13. TROUBLESHOOTING

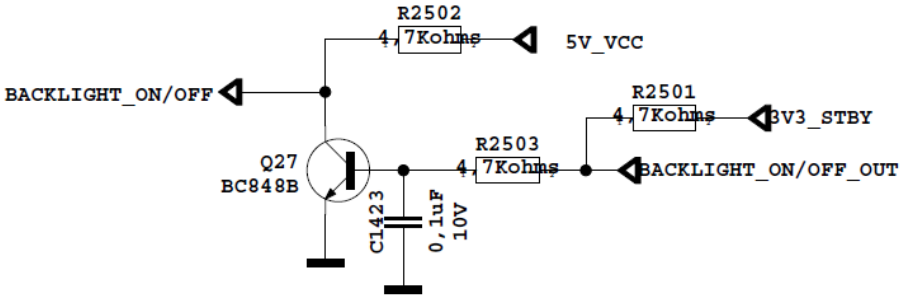
A. NO BACKLIGHT PROBLEM

Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible causes: Backlight pin, dimming pin, backlight supply (Panel_VCC), stby on/off pin

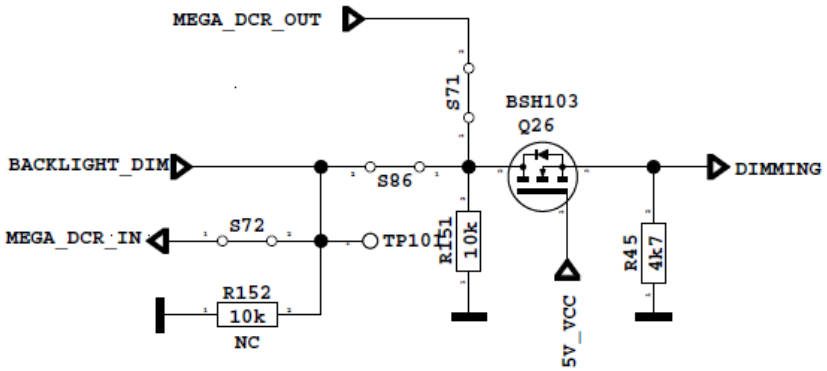
BACKLIGHT_ON/OFF pin should be high when the backlight is ON. Collector pin of Q27 must be low when the backlight is OFF. If it is a problem, please check Q27 and the panel cables. Also it can be tested in TP244 in main board.

Backlight On/Off Circuit

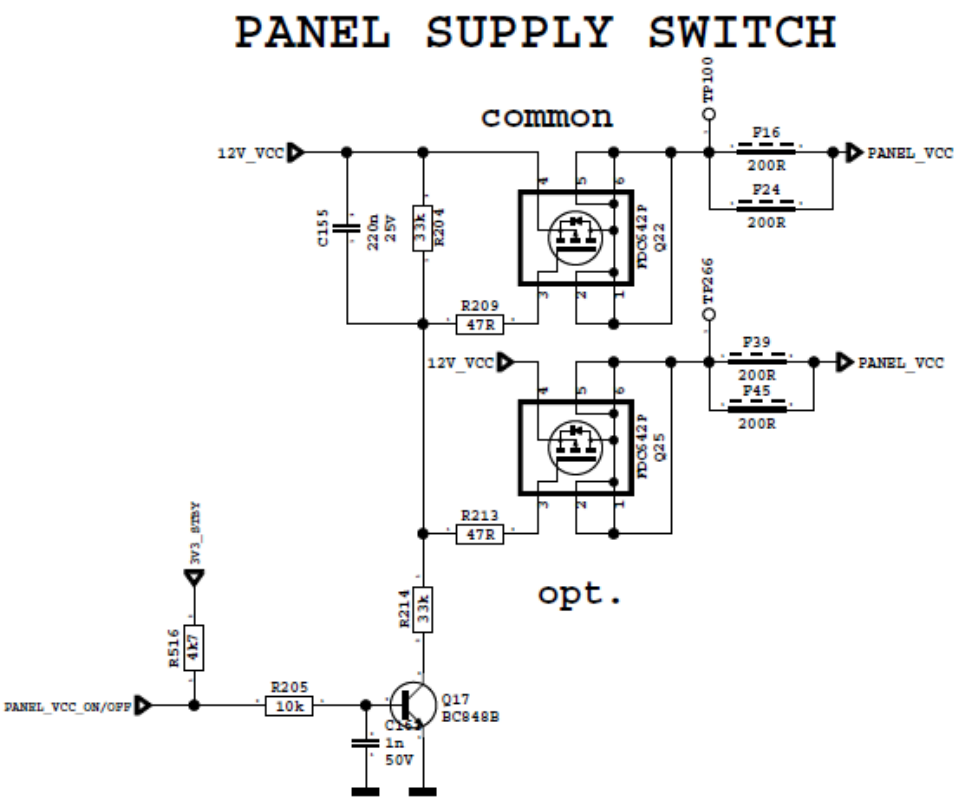


Dimming pin should be high or square wave in open position. If it is low, please check S86 for Novatek side and panel or power cables, connectors.

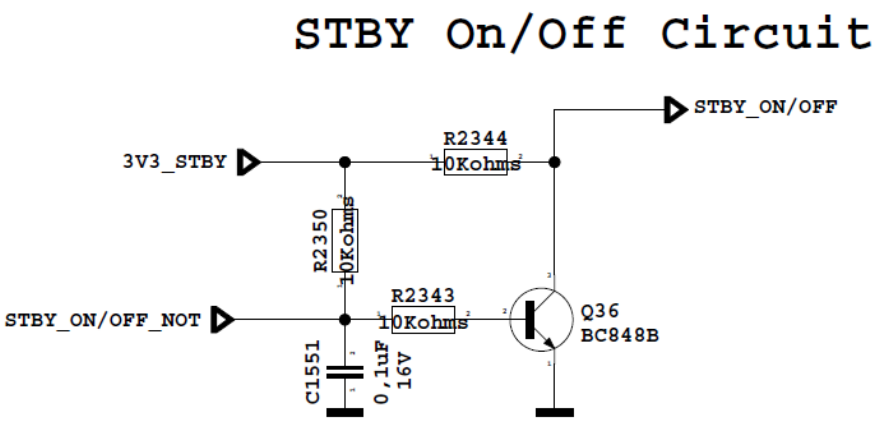
DIMMING



Backlight power supply (Panel_VCC) should be in panel specs. Please check Q22, Q25, shown below; also it can be checked TP100.



STBY_ON/OFF should be low for TV on condition, please check Q36's collector.

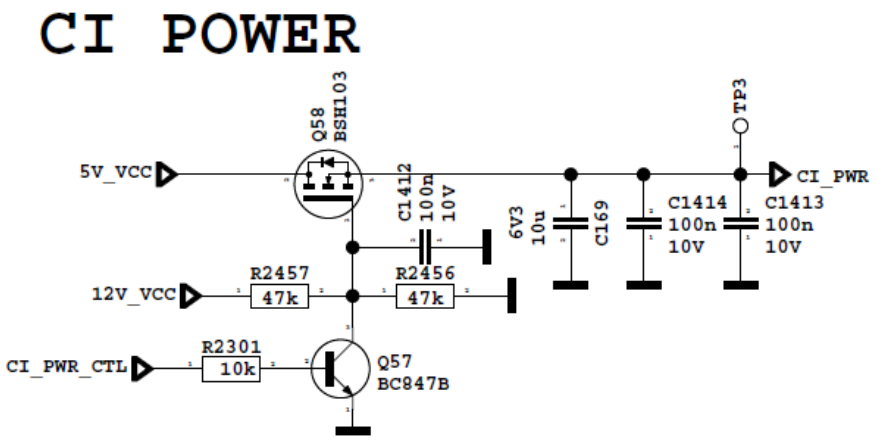


B. CI MODULE PROBLEM

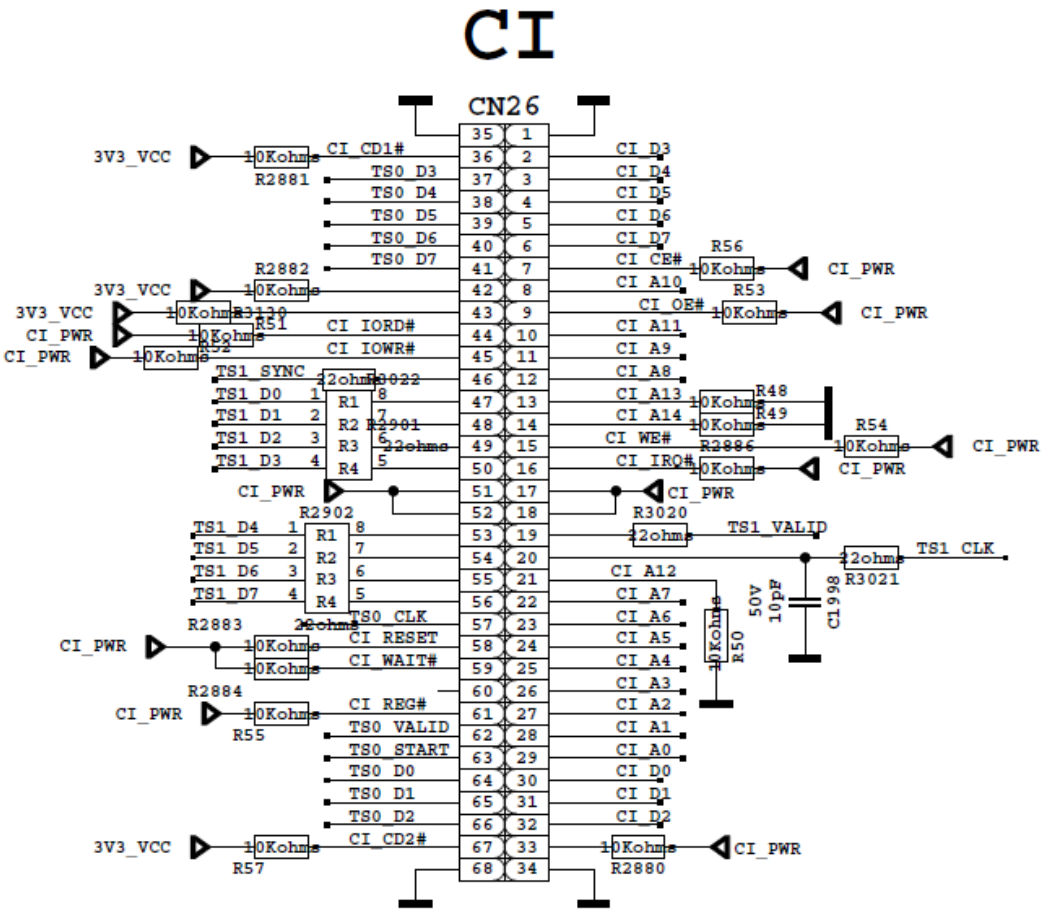
Problem: CI is not working when CI module inserted.

Possible causes: Supply, suply control pin, detects pins, mechanical positions of pins.

- CI supply should be 5V when CI module inserted. If it is not 5V please check CI_PWR_CTL, this pin should be low.



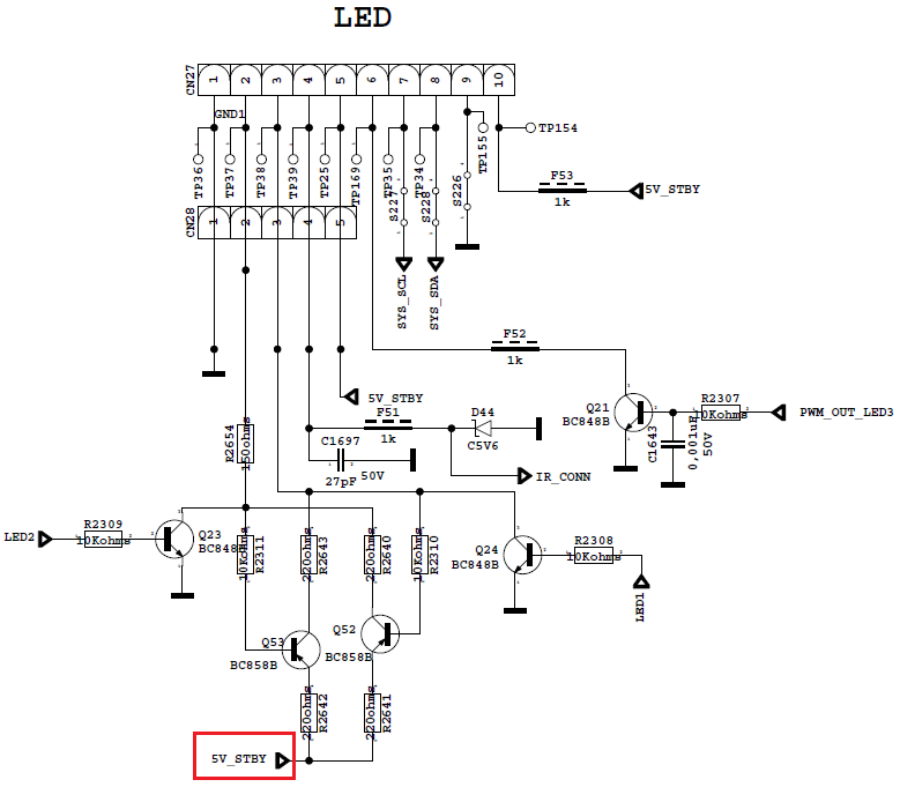
- Please check mechanical position of CI module. Is it inserted properly or not?
- Detect ports should be low. If it is not low please check CI connector pins, CI module pins.



C. IR PROBLEM

Problem: LED or IR not working

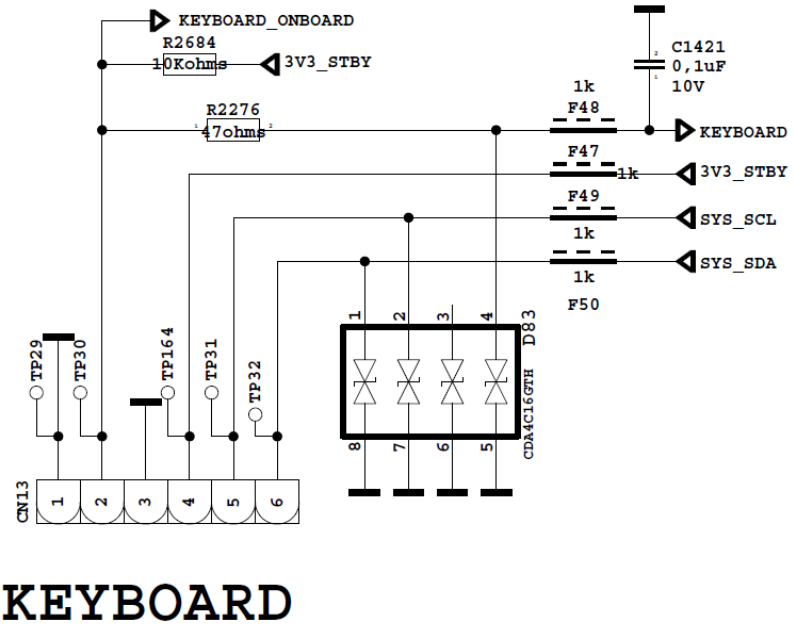
Check LED card supply on MB230 chasis.



D. KEYPAD TOUCHPAD PROBLEMS

Problem: Keypad or Touchpad is not working

Check keypad supply on MB230.

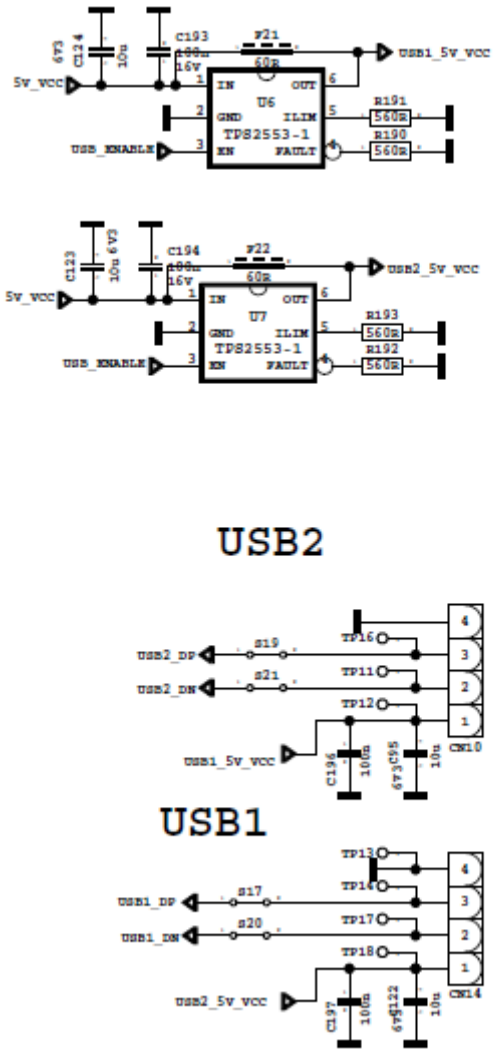


KEYBOARD

E. USB PROBLEMS

Problem: USB is not working or no USB Detection.

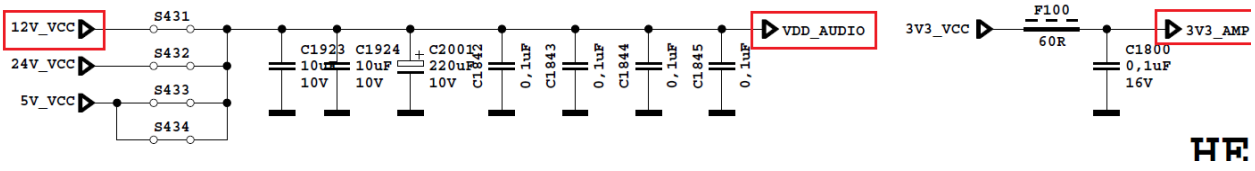
Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.

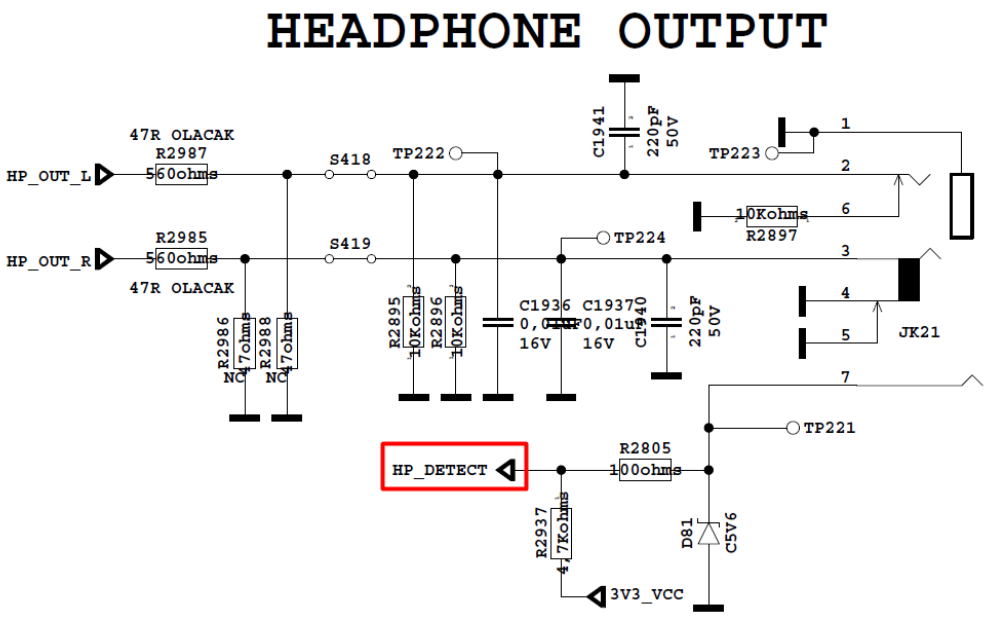


F. NO SOUND PROBLEM

Problem: No audio at main TV speaker outputs.

Check supply voltages of 12V_VCC, VDD_AUDIO and 3V3_AMP with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3v.





G. STANDBY ON/OFF PROBLEM

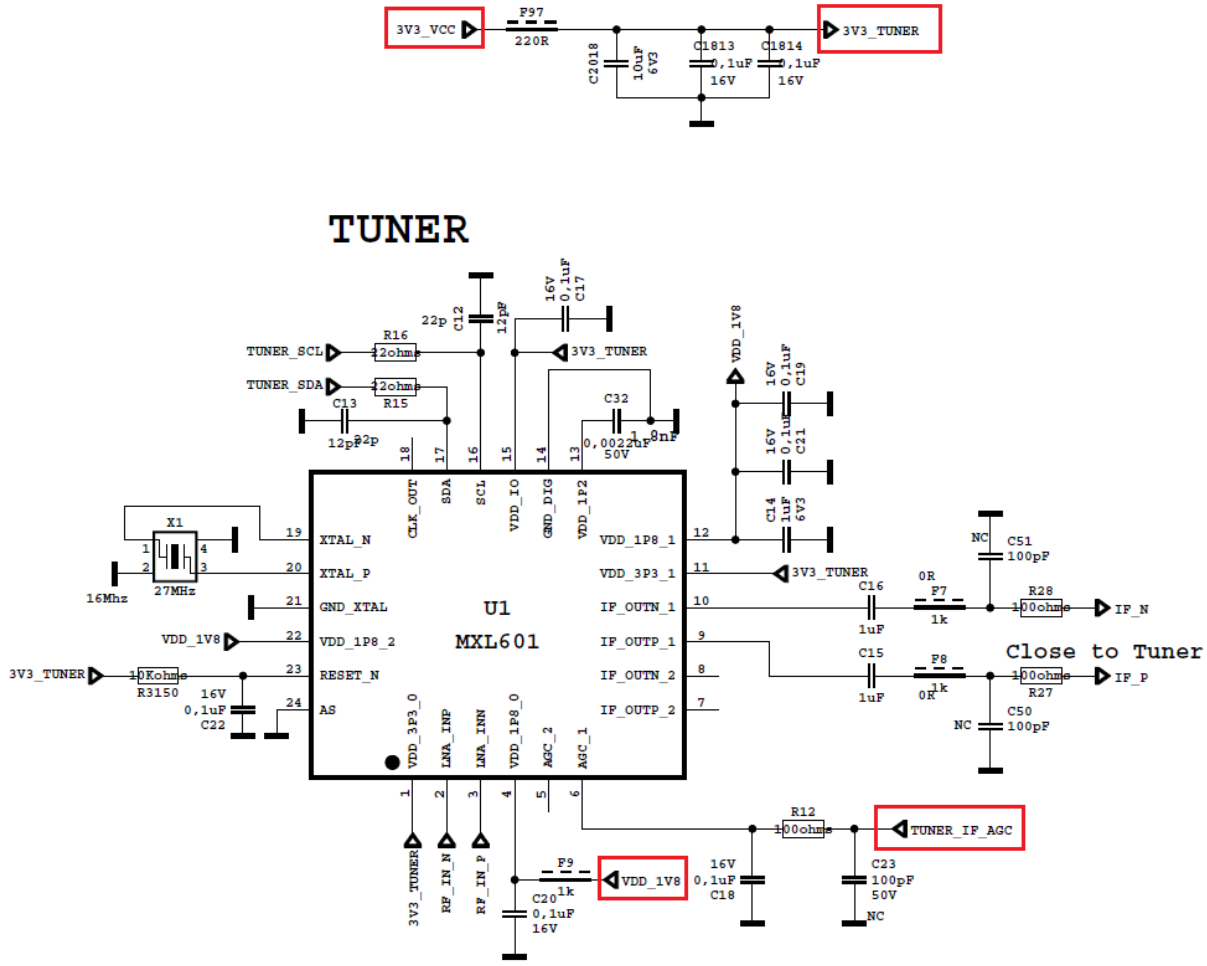
Problem: Device can not boot, TV hangs in standby mode.

There may be a problem about power supply. Check main supplies with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via Teraterm. These printouts may give a clue about the problem. You can use VGA for terraterm connection.

H. NO SIGNAL PROBLEM

Problem: No signal in DVB-T/T2/C mode.

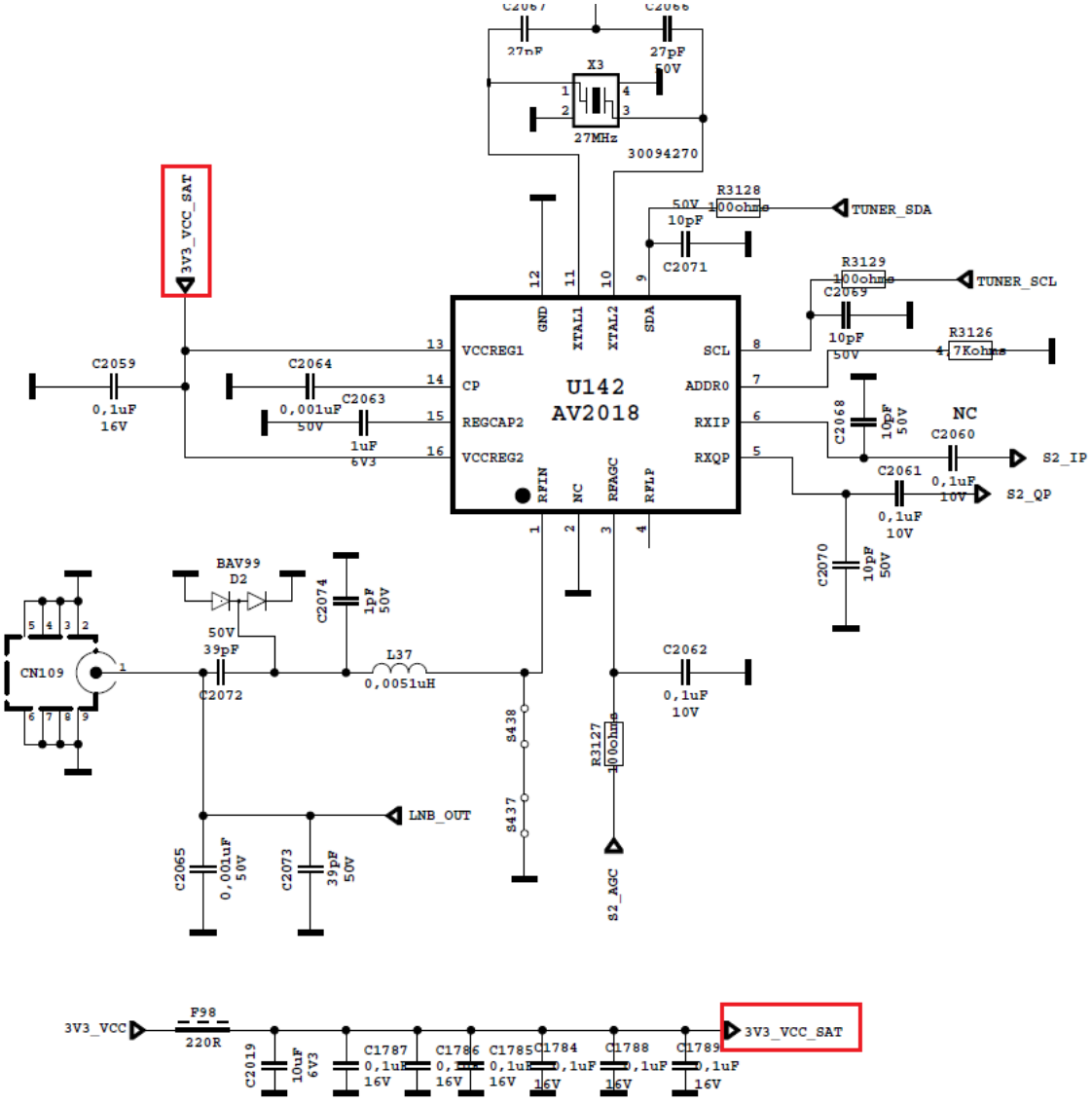
Check tuner supply voltage; 3V3_TUNER and VDD_1V8. Check tuner options are correctly set in Service menu. Check AGC voltage at TUNER_IF_AGC pin of tuner.



Problem: No signal or Low signal in DVB-S/S2 mode.

Check signal cables and LNB voltage, if there is no problem, check AV2018 supply voltage 3V3_VCC_SAT. If it is OK, then measure the voltage from the PIN1 of U142.

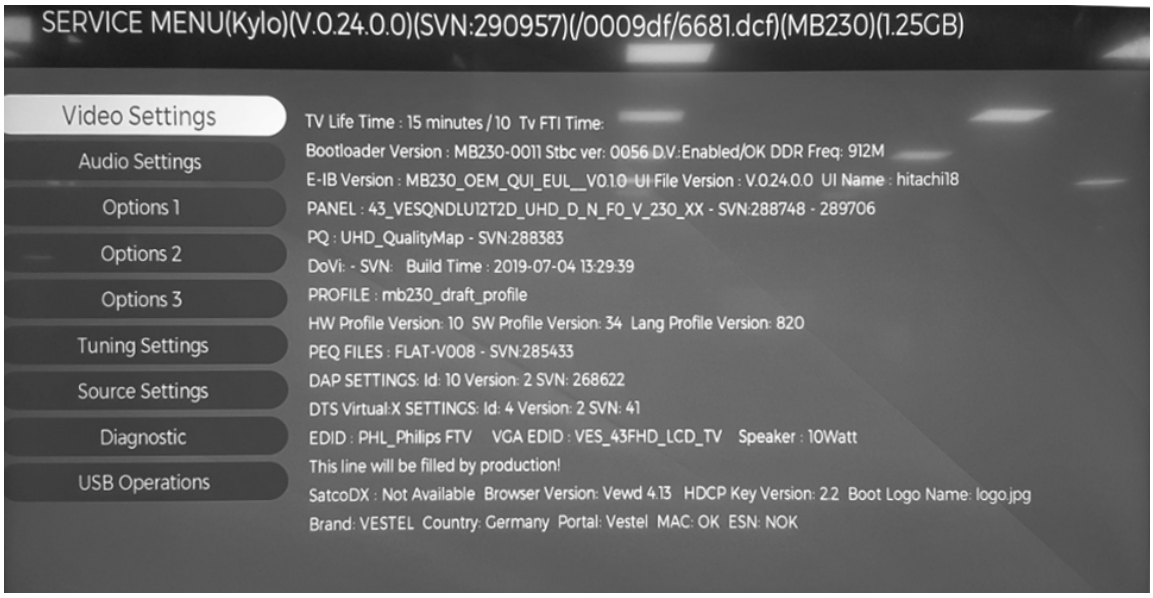
If the PIN1 voltage is equal to 0V, please check i2c waveforms and software. If the PIN1 voltage is lower than 1V (e.g: 0.8Vor 0.3V), change the U142 with a new part.


X3
27MHz
30094270
27pF
50V
3V3_VCC_SAT
R3128
100ohms
TUNER_SDA
C2071
10pF
R3129
100ohms
TUNER_SCL
C2069
10pF
50V
R3126
7Kohms
U142
AV2018
GND
XTAL1
XTAL2
SDA
SCL
ADDR0
RXIP
RXQP
VCCREG1
CP
REGCAP2
VCCREG2
RFIN
NC
RFAGC
RFLP
C2059
0,1uF
16V
C2064
0,001uF
50V
C2063
1uF
6V3
C2068
10pF
50V
NC
C2060
S2_IP
C2061
0,1uF
10V
S2_QP
0,1uF
10V
C2070
10pF
50V
BAV99
D2
C2074
1pF
50V
CN109
50V
39pF
C2072
L37
0,0051uH
C2062
0,1uF
10V
S438
S437
R3127
100ohms
LNB_OUT
C2065
0,001uF
50V
C2073
39pF
50V
S2_AGC
3V3_VCC
F98
220R
C2019
10uF
6V3
C1787
0,1uF
16V
C1786
0,1uF
16V
C1785
0,1uF
16V
C1784
0,1uF
16V
C1788
0,1uF
16V
C1789
0,1uF
16V
3V3_VCC_SAT

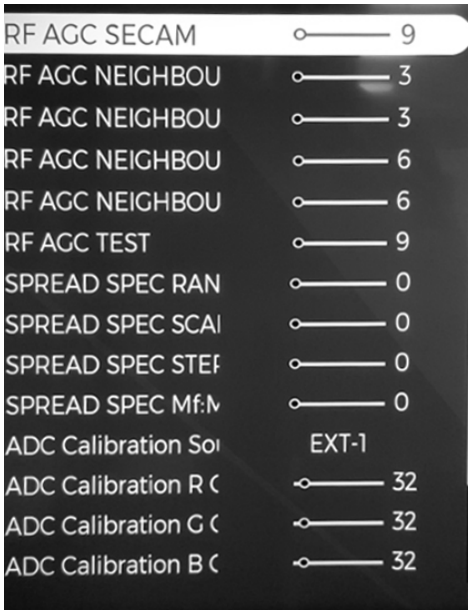
14. SERVICE MENU SETTINGS

In order to reach service menu, first Press **"MENU"** buton, then write "**4725"** by using remote controller.

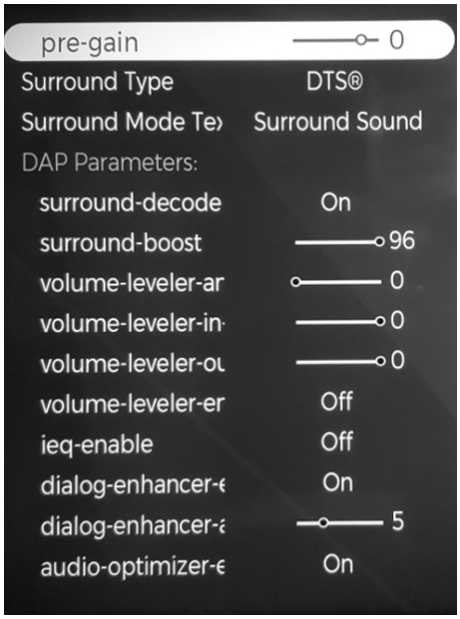
You can see the service menu main screen below. You can check SW releases by using this menu. In addition, you can make changes on video, audio etc. by using video settings, audio settings titles.



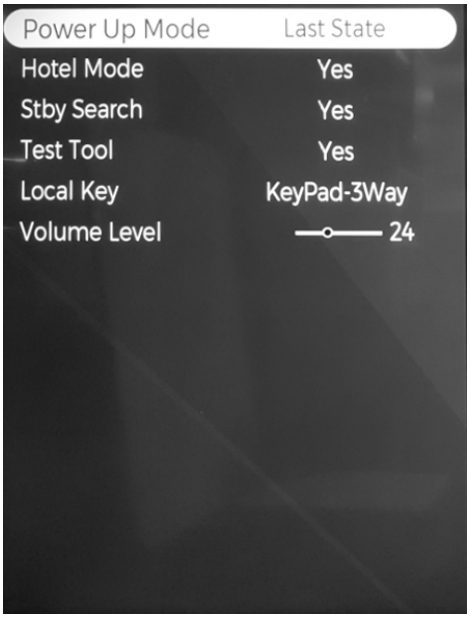
Service Menu Main Screen



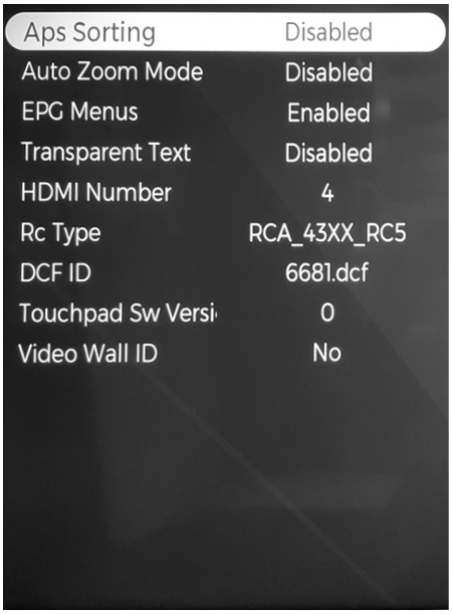
Video Settings



Audio Settings

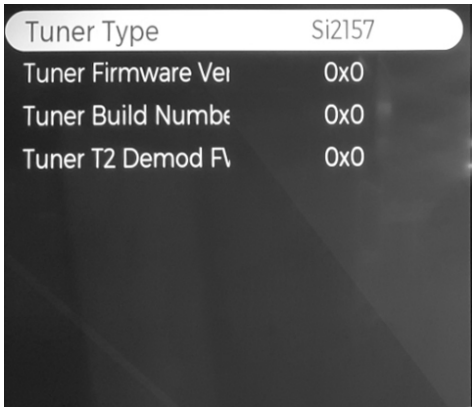


Options-1 Menu

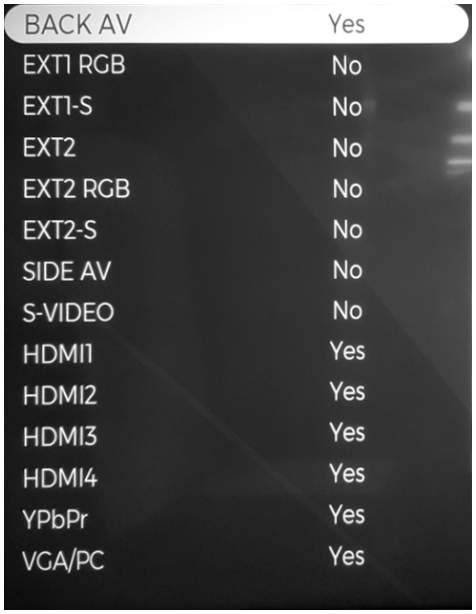


Options-2 Menu

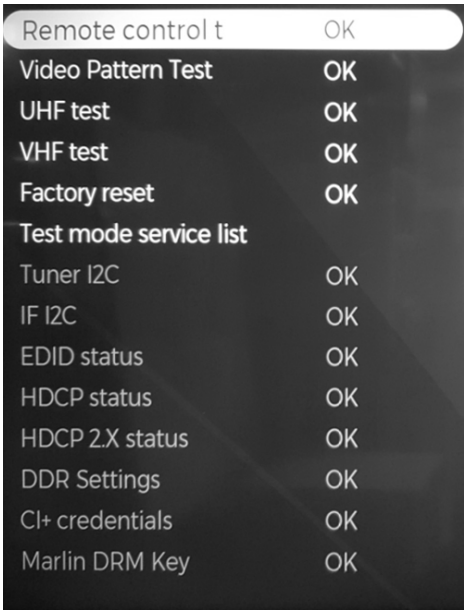
Options-3 Menu



Tuner Settings Menu

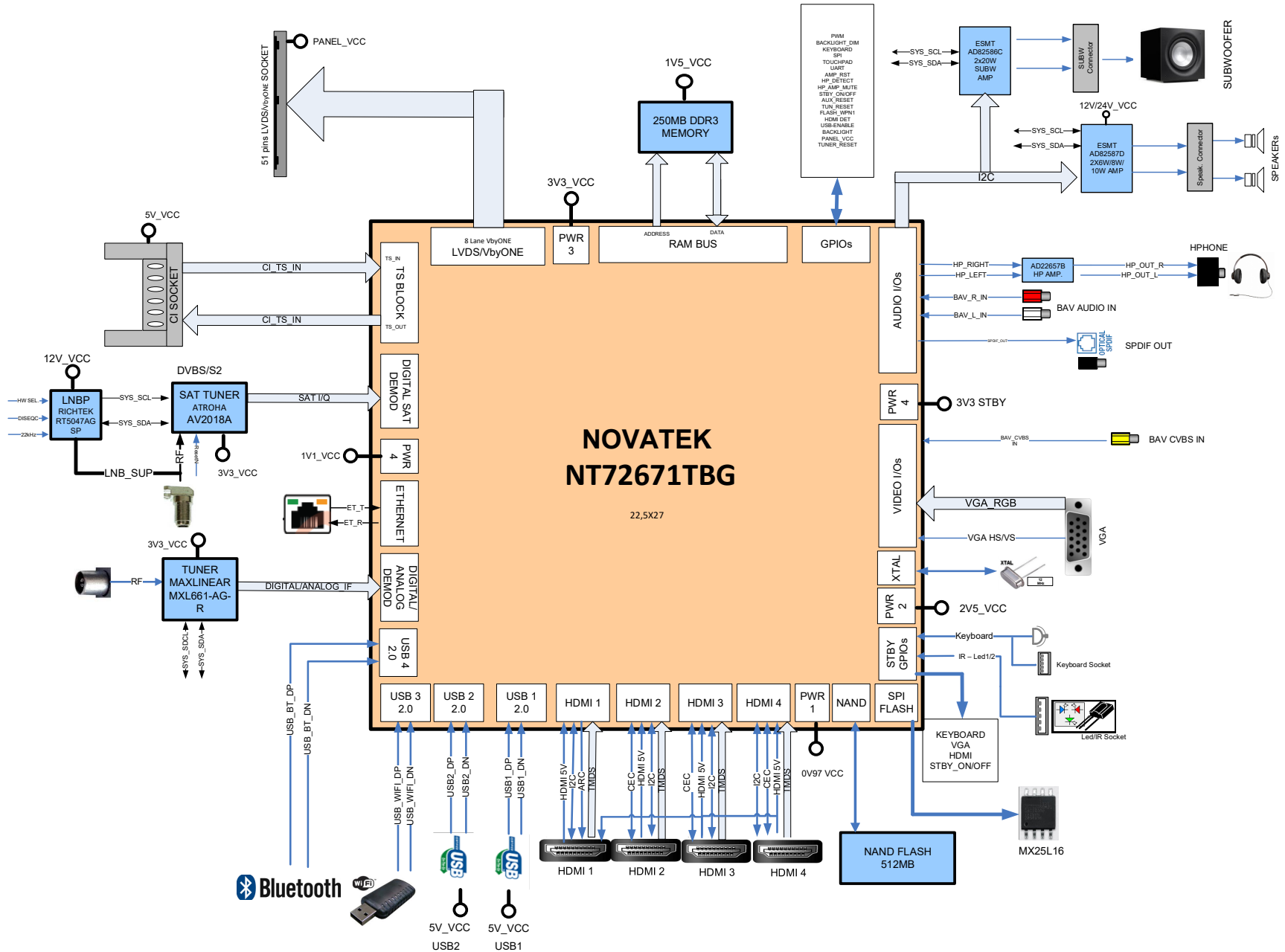


Source Settings Menu



Diagnostic Menu

15.GENERAL BLOCK DIAGRAM



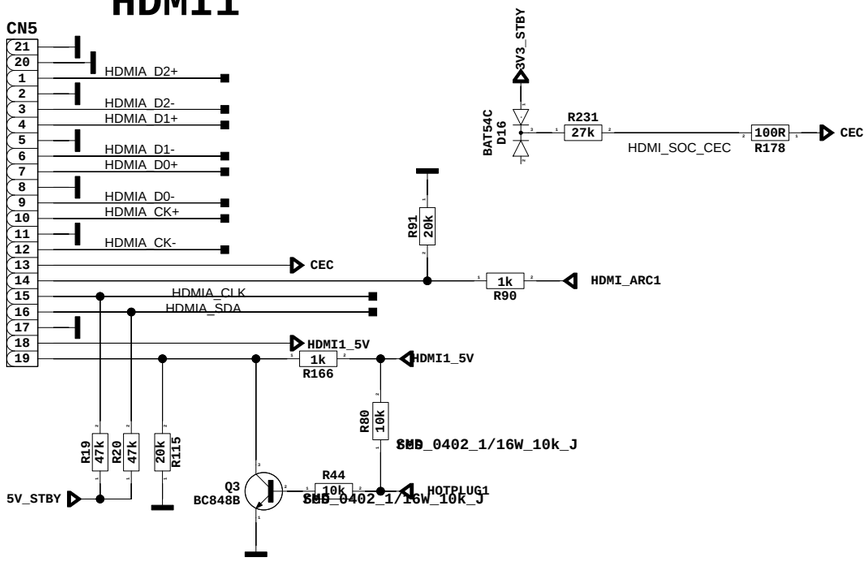
DQ0 VE DQ2 LAYOUTTA KONTROL EDILECEK(swap EDILEB

VDD15_DDR_M

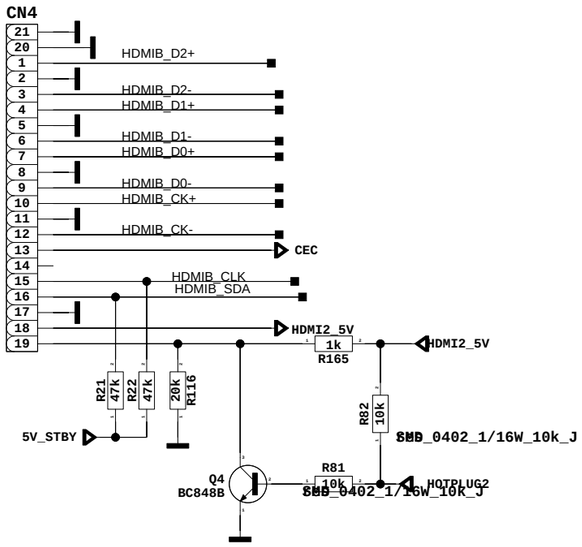
VDD15_DDR_M

VDD15_DDR_M

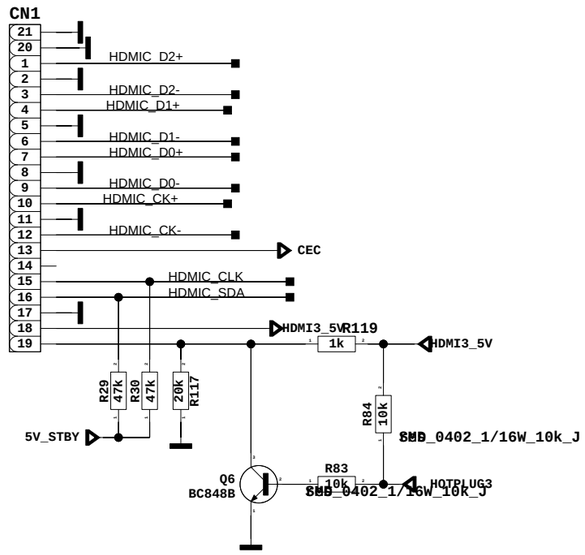
HDMI1

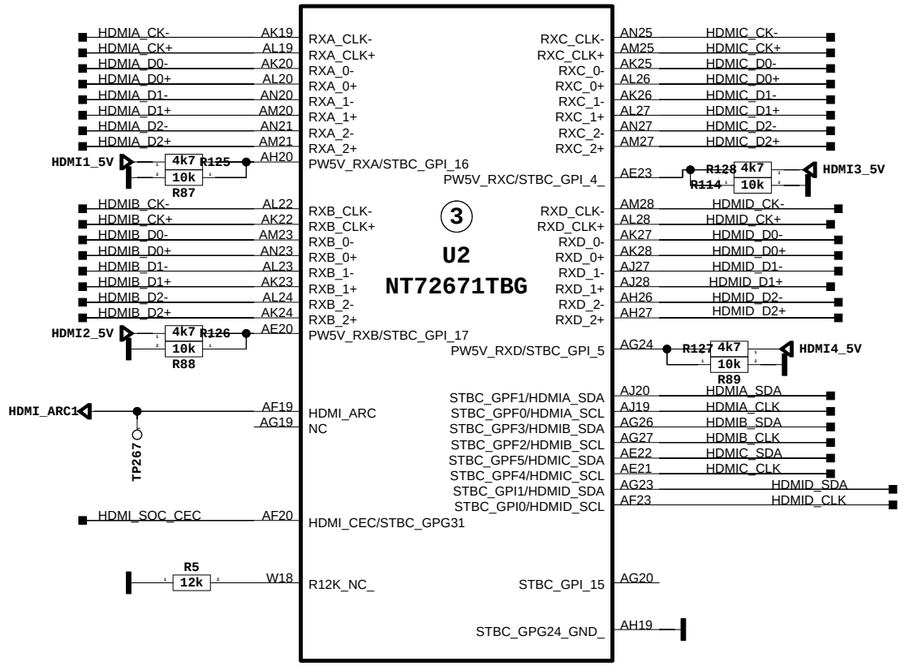


HDMI2

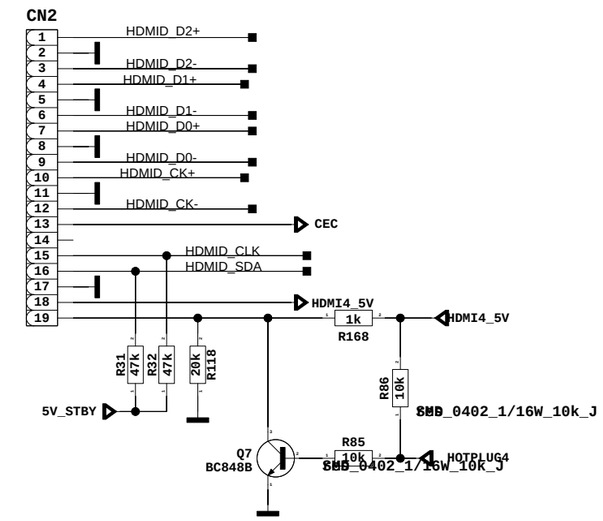


HDMI3





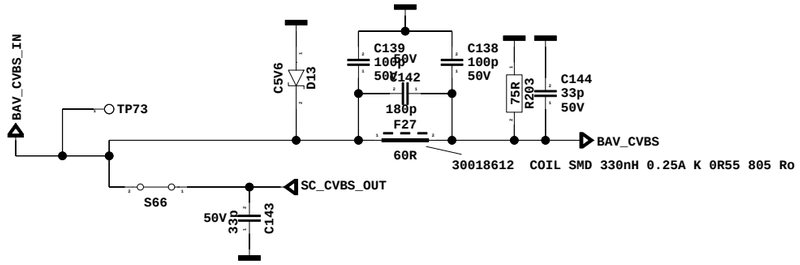
HDMI4



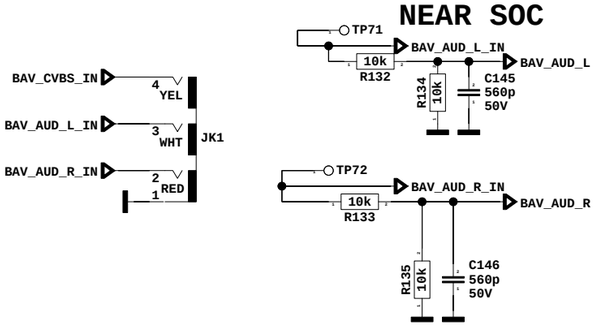
VESTEL	PROJECT NAME : 17mb230-r2	A3
SCH NAME :HDMI	T. SHT	15
DRAWN BY :<YOUR NAME HERE>	14/03/2019:10:24	

4.7Kohms

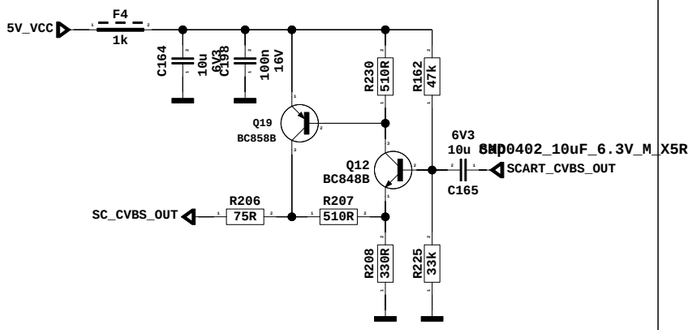
BAV-IN

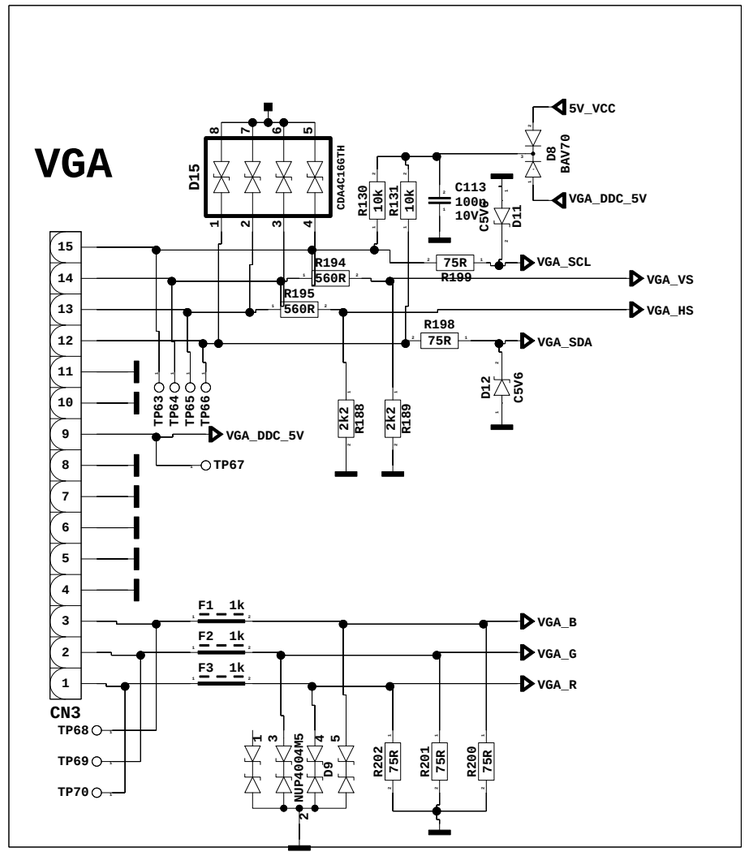


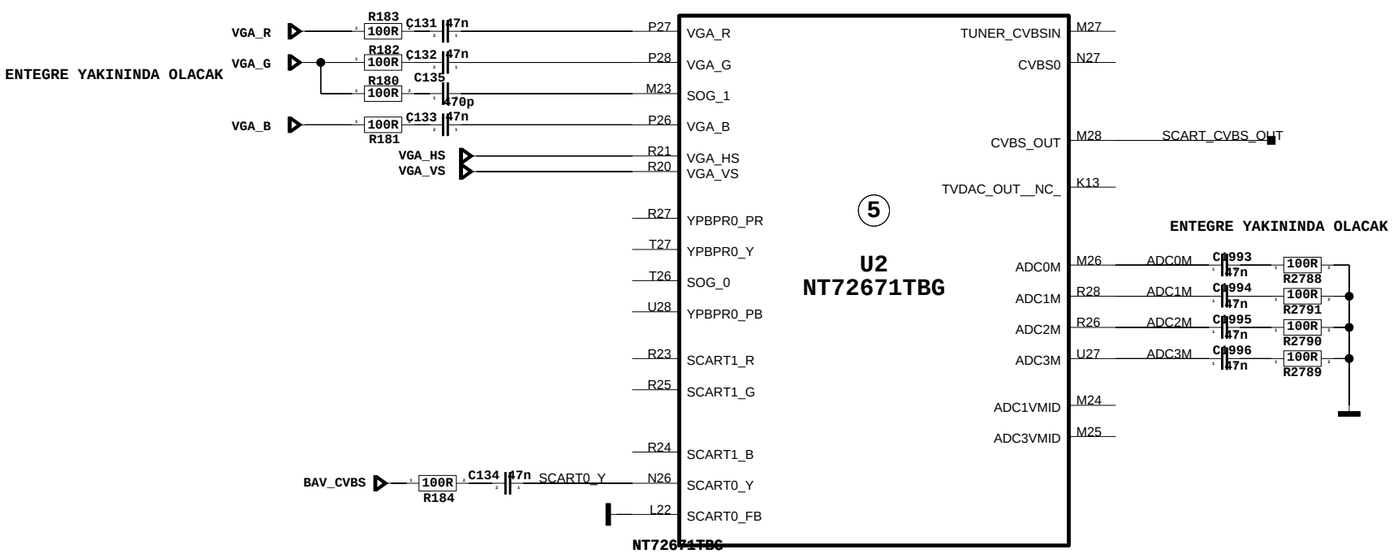
NEAR SOC



CVBS VIDEO OUTPUT AMPLIFIER

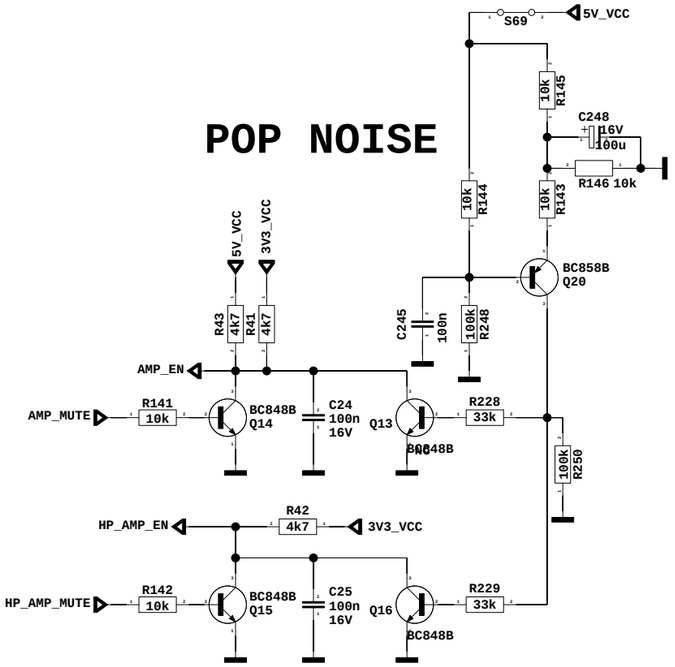




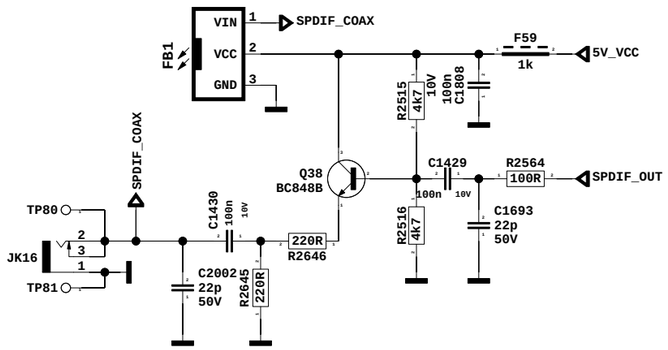


VESTEL	PROJECT NAME :17mb230-r2	A3
SCH NAME :PERIPHERALS		T. SHT 15
DRAWN BY :<YOUR NAME HERE>		11/03/2019:14:09

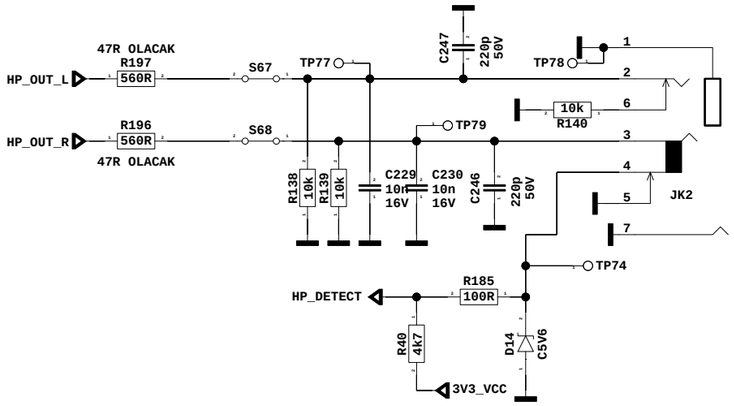
POP NOISE



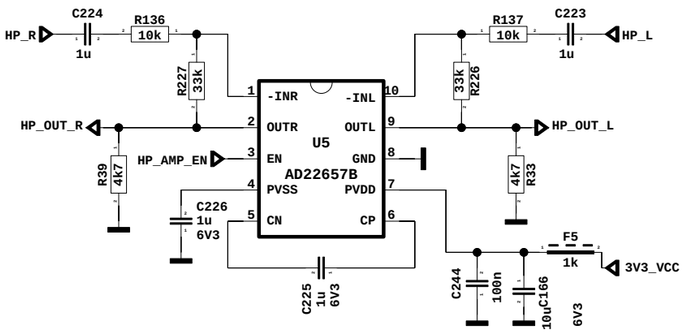
SPDIF OUT



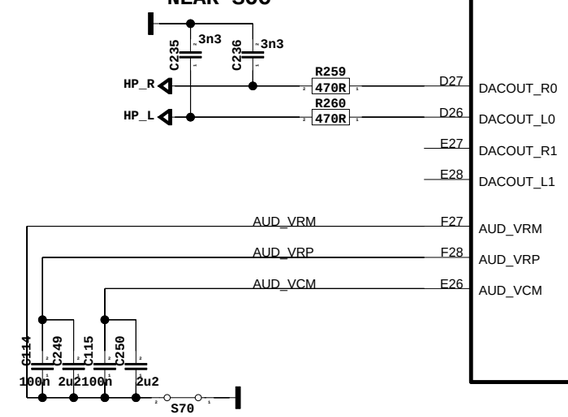
HEADPHONE OUTPUT

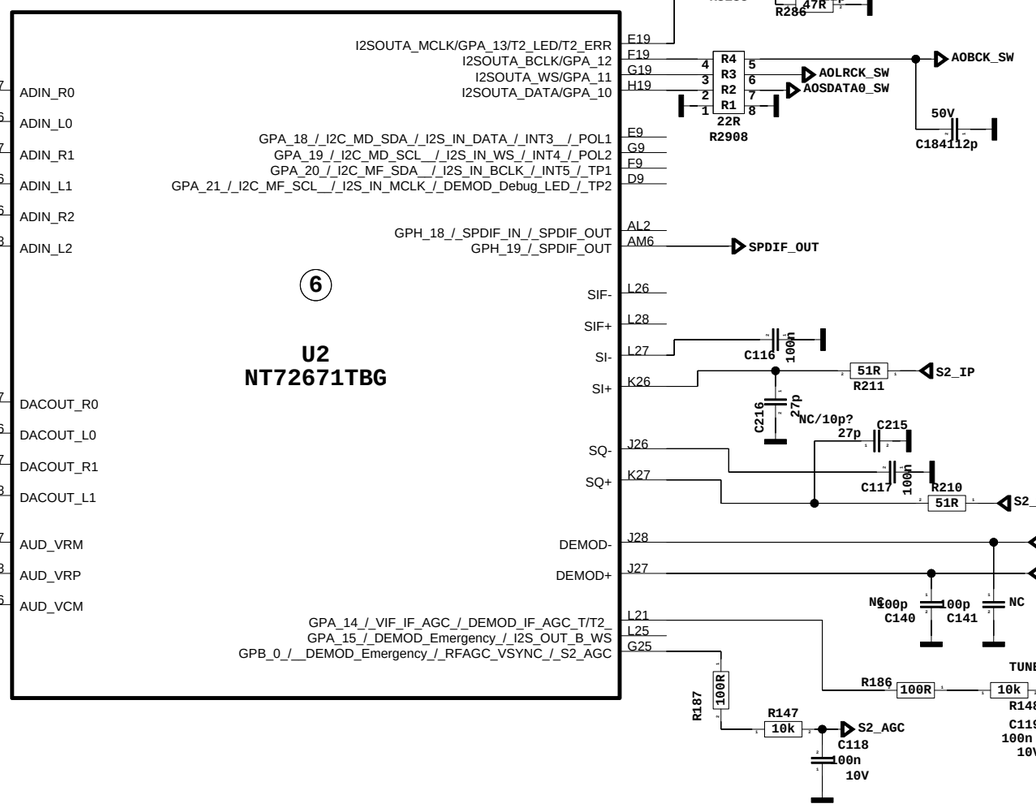


HEADPHONE AMP



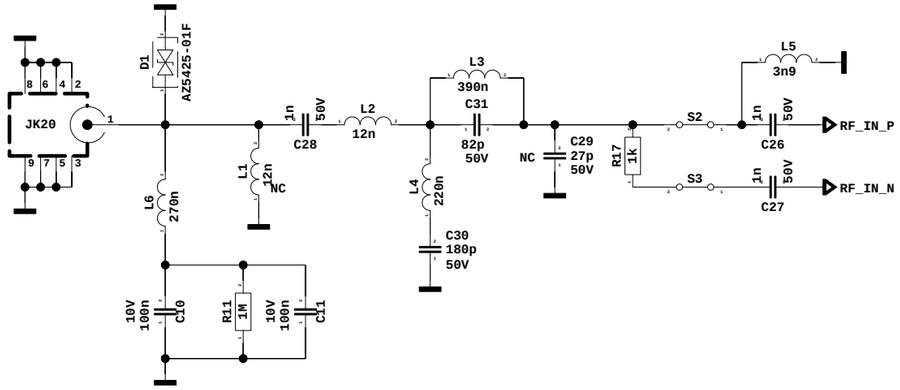
NEAR SOC

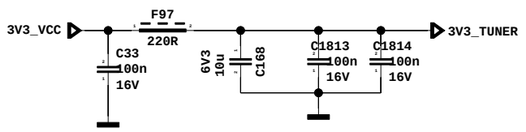




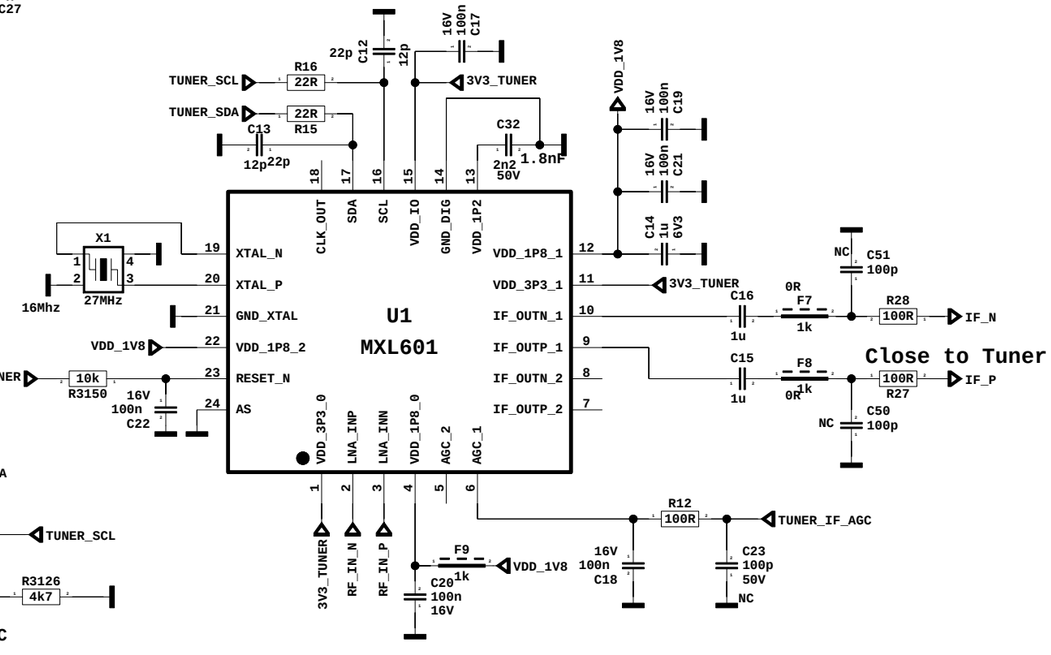
VESTEL	PROJECT NAME : 17mb230-r2		A3
SCH NAME :AUDIO DEMOD		T. SHT	15
DRAWN BY :<YOUR NAME HERE>		11/03/2019:14:09	

TUNER

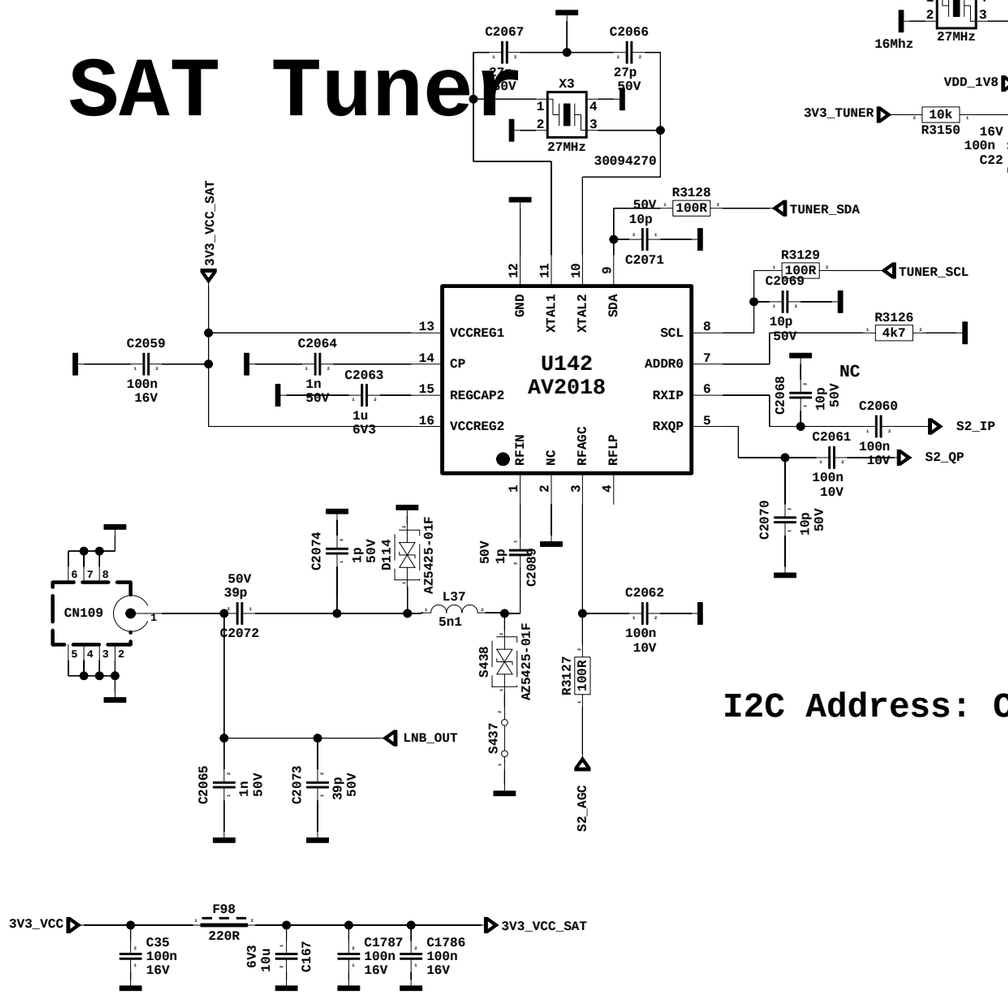




TUNER

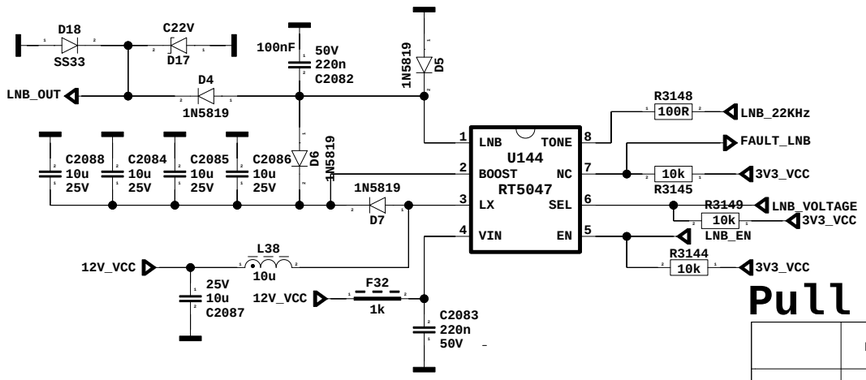


SAT Tuner



I2C Address: C4

LNBP

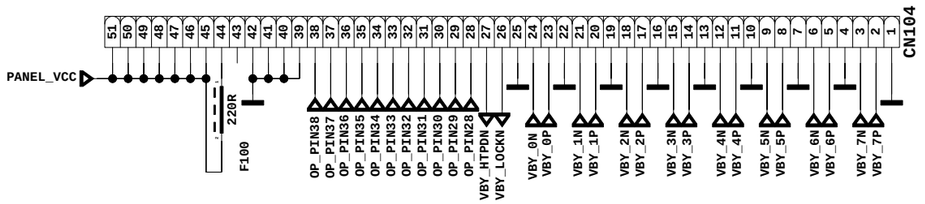


Pull up/Pull do

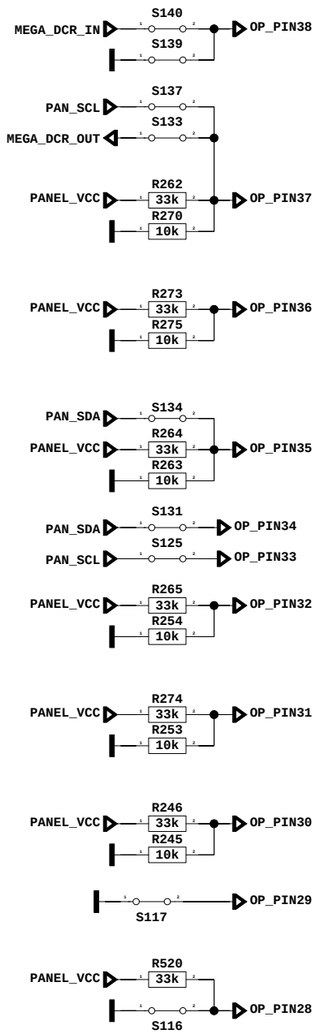
	LNB_VOLTAGE	LNB_EN
HIGH	18V	ENABLE
LOW	13V	DISABLE

VESTEL	PROJECT NAME :17mb230-r2	A3
SCH NAME :TUNER		T. SHT15
DRAWN BY :<YOUR NAME HERE>		11/03/2019:14:09

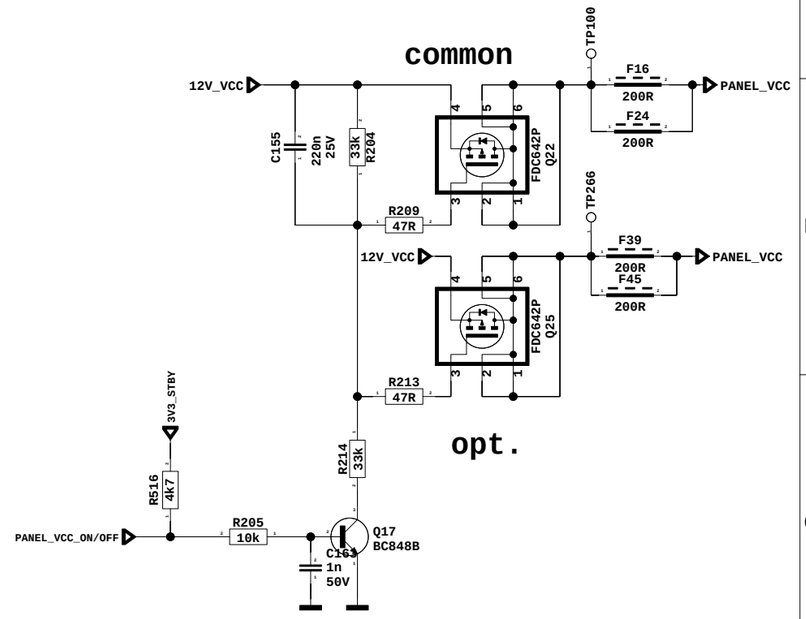
VBYONE SOCKET



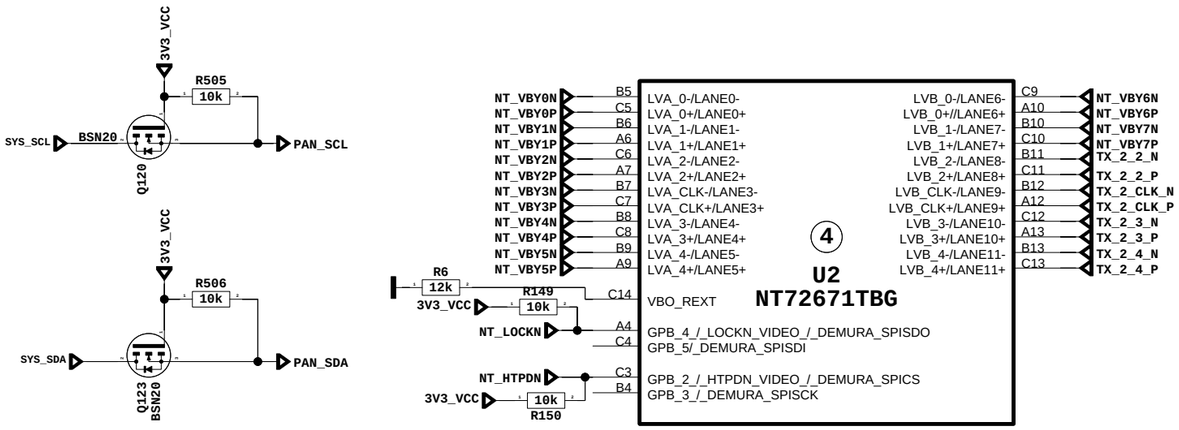
OPTIONS TABLE



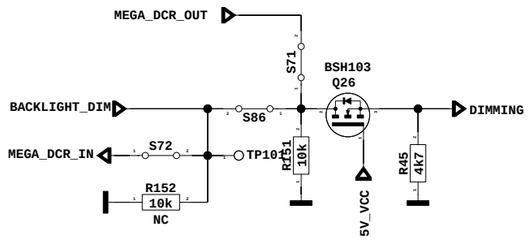
PANEL SUPPLY SWITCH



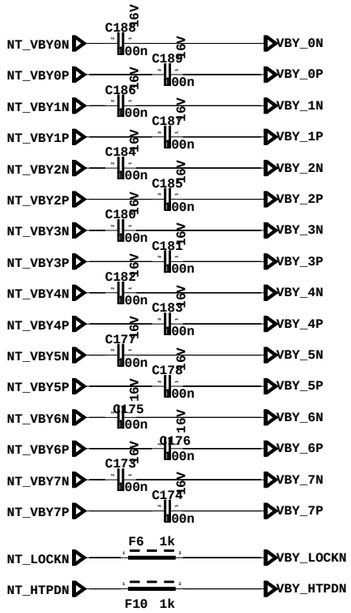
PANEL I2C BUFFER



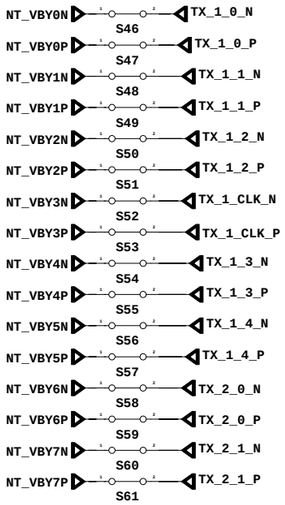
DIMMING



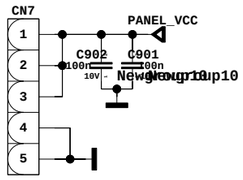
Vby1 OPTION



LVDS OPTION

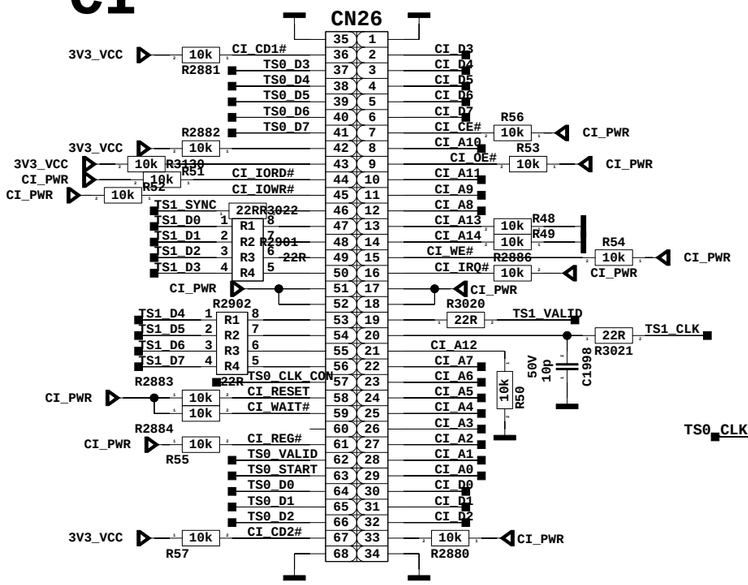


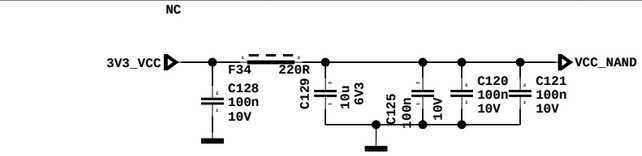
65LG_VCC

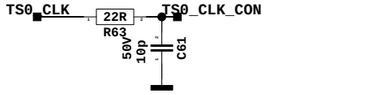


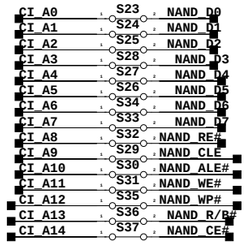
VESTEL	PROJECT NAME : 17mb230-r2	A3
SCH NAME :VBYONE		T. SHT 15
DRAWN BY :<YOUR NAME HERE>		26/03/2019:14:29

CI

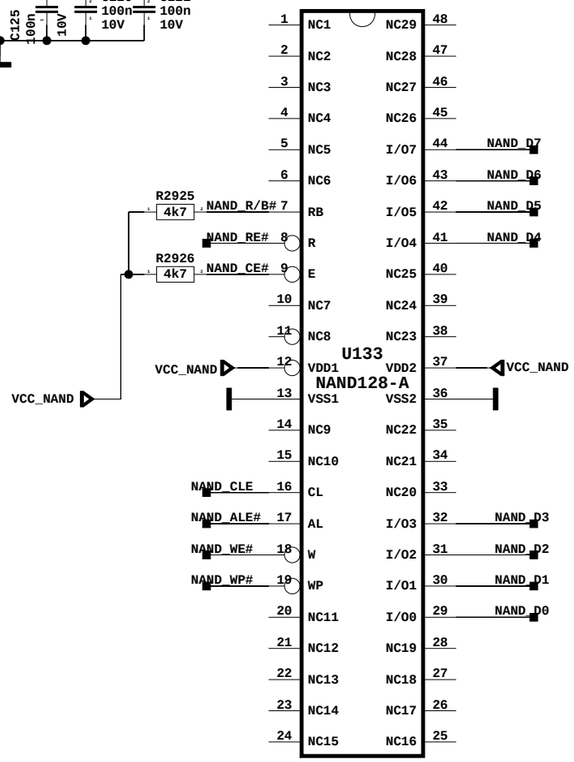




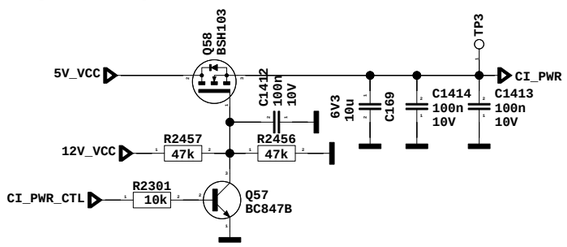


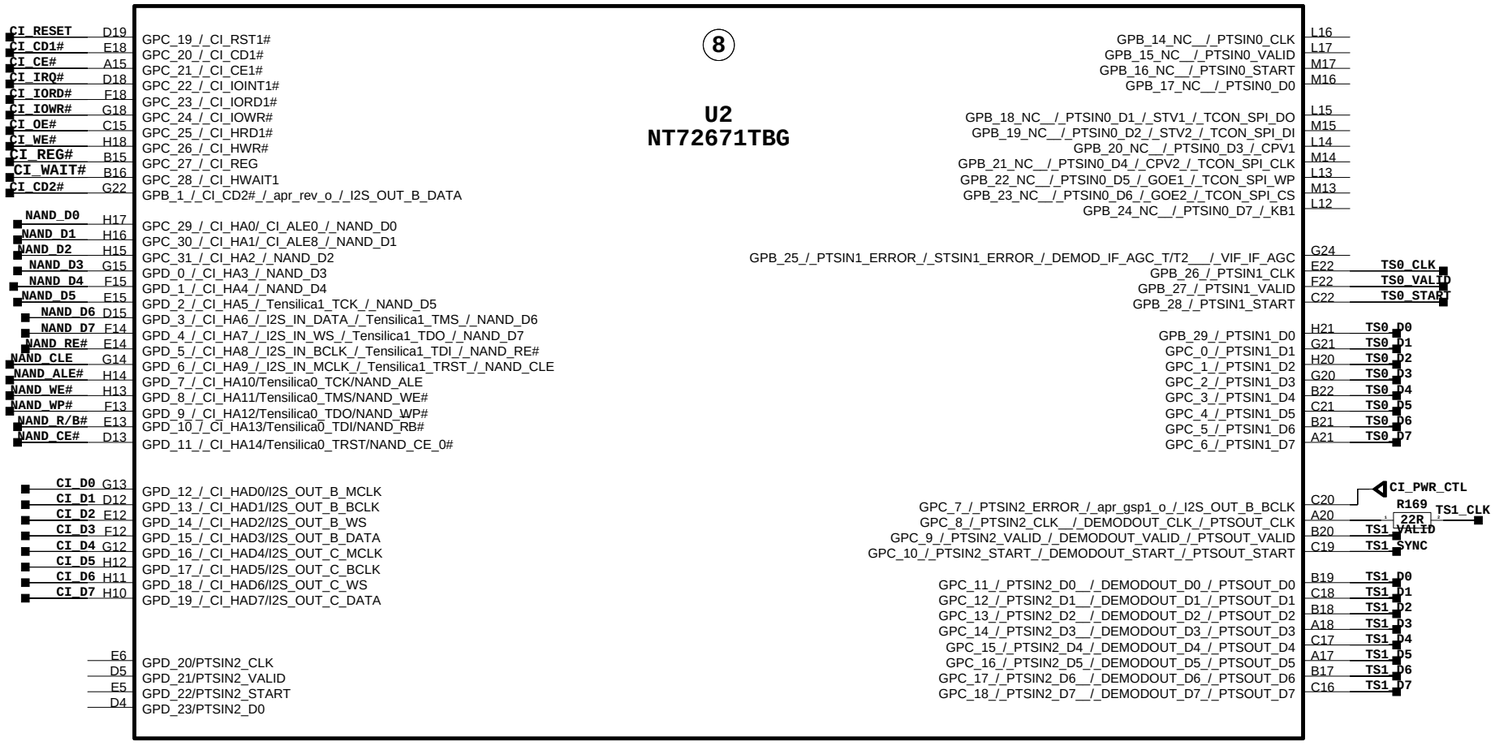


NAND FLASH

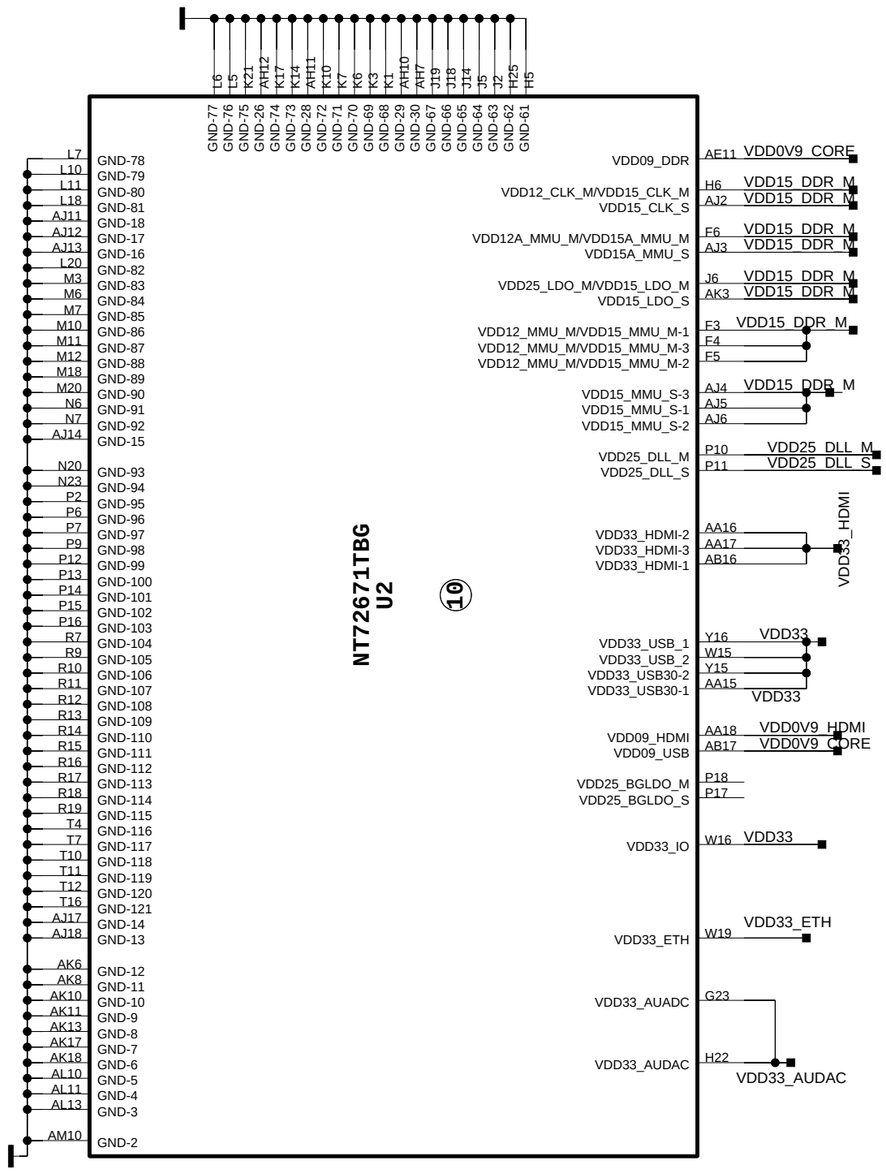


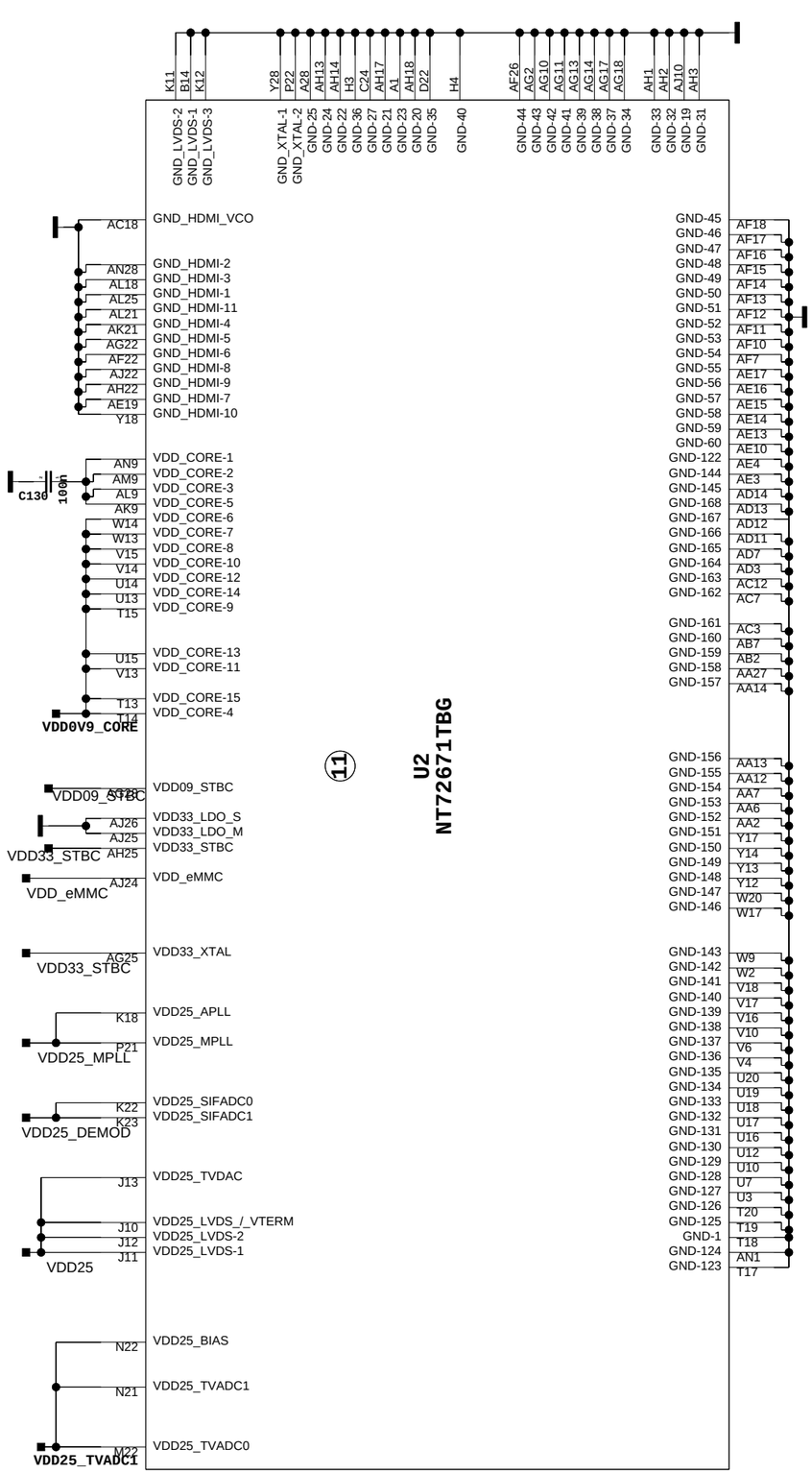
CI POWER

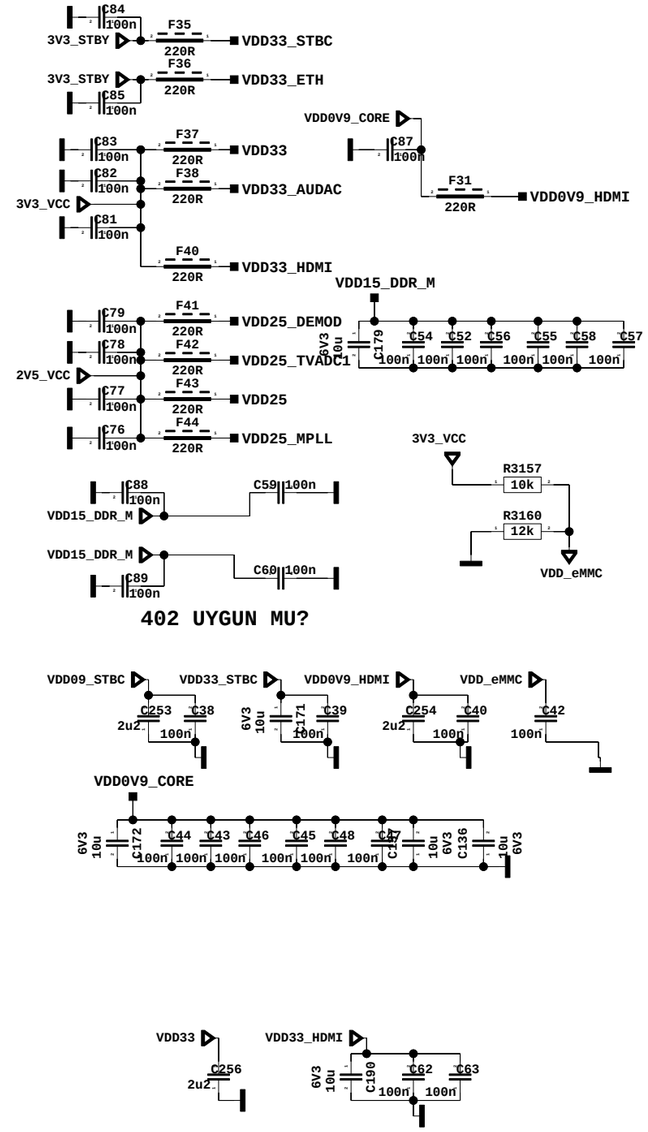


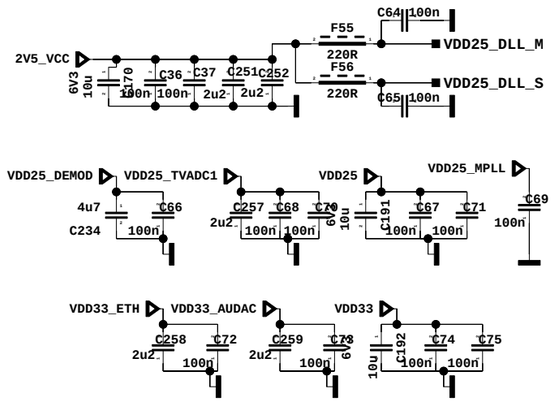


VESTEL	PROJECT NAME : 17mb230-r2		A3
	SCH NAME :CI/NAND	T. SHT	15
	DRAWN BY :<YOUR NAME HERE>	11/03/2019:14:09	



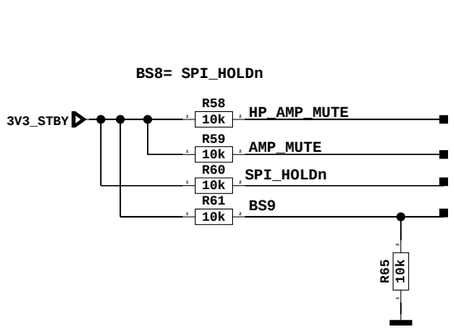


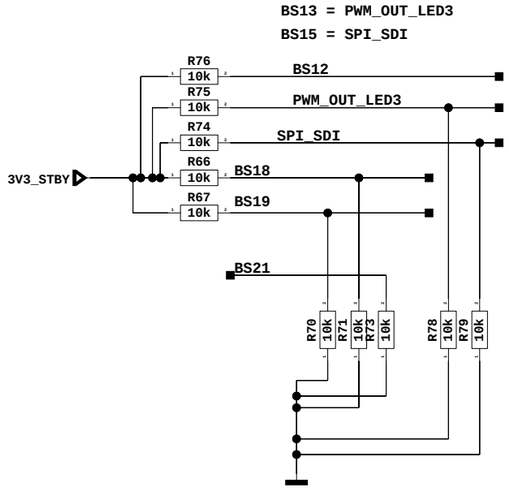




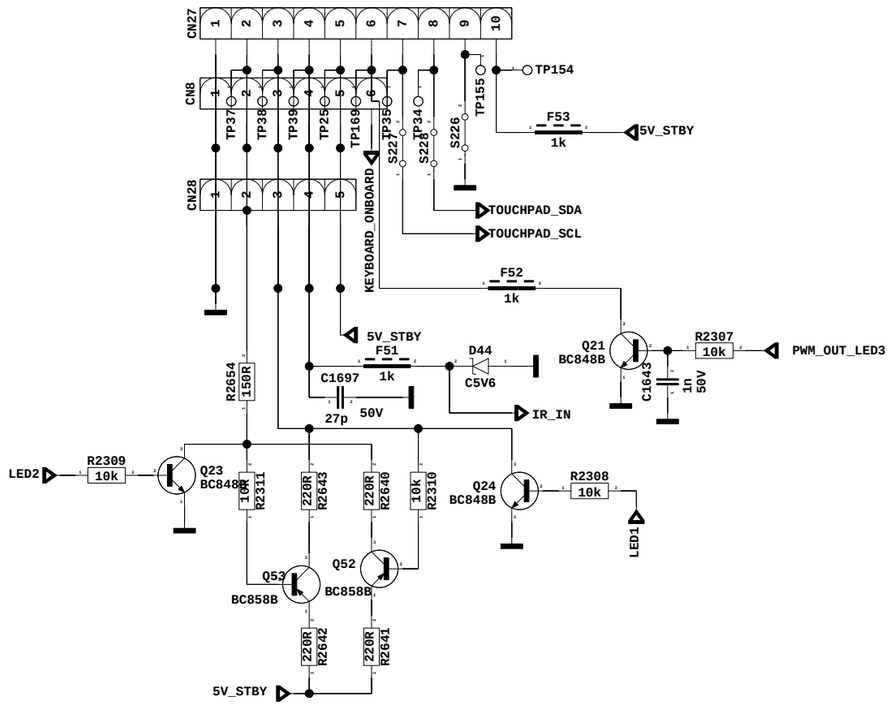
VESTEL	PROJECT NAME : 17mb230-r2	A3
SCH NAME :SOC_POWER		T. SHT 15
DRAWN BY :<YOUR NAME HERE>		11/03/2019:14:09

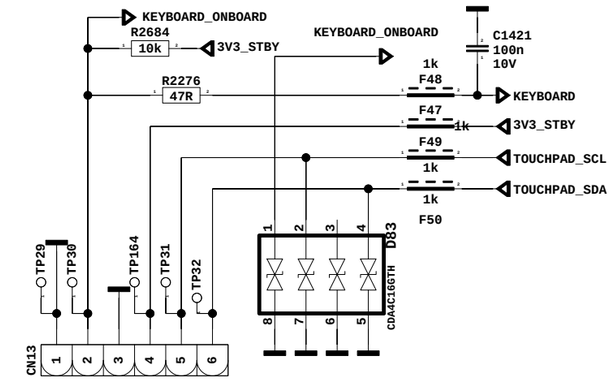
BOOTSTRAP





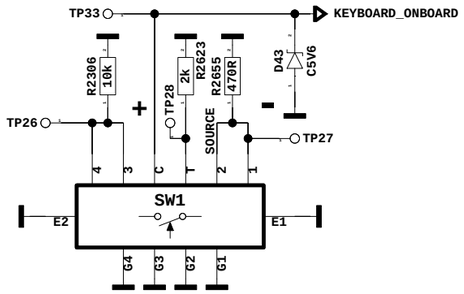
LED



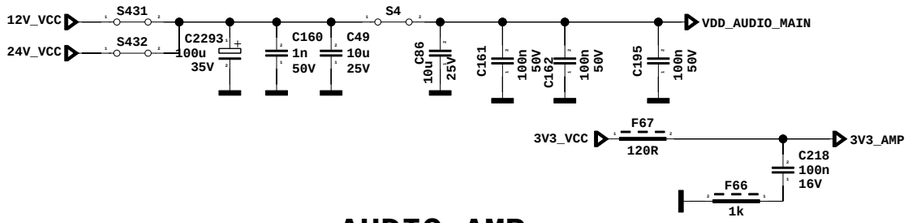


KEYBOARD

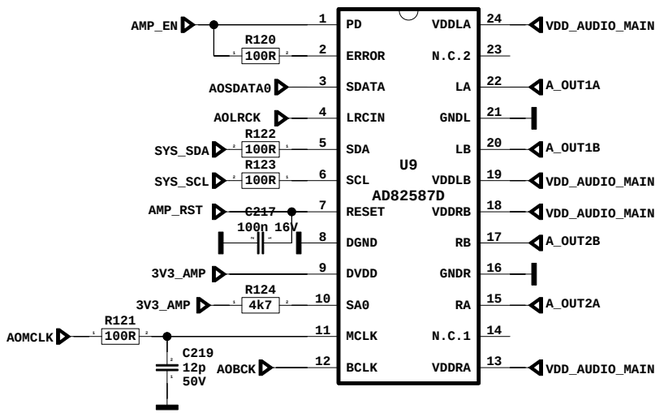
3-WAY

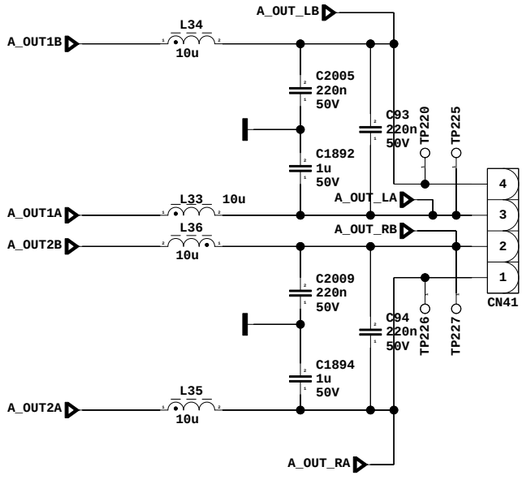


VESTEL	PROJECT NAME : 17mb230-r2	A3
SCH NAME :GPIOs		T. SHT 15
DRAWN BY :<YOUR NAME HERE>		11/03/2019:14:09

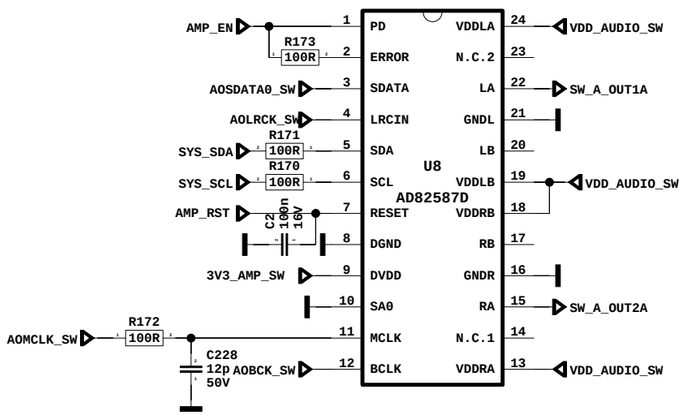


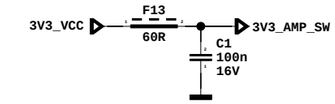
AUDIO AMP

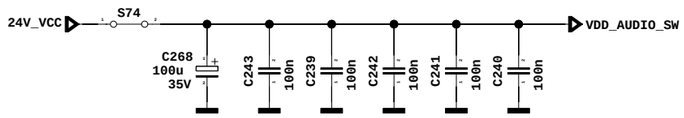


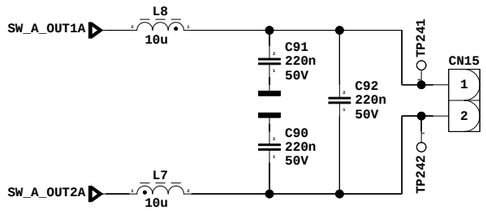


SUBWOOFER AMP

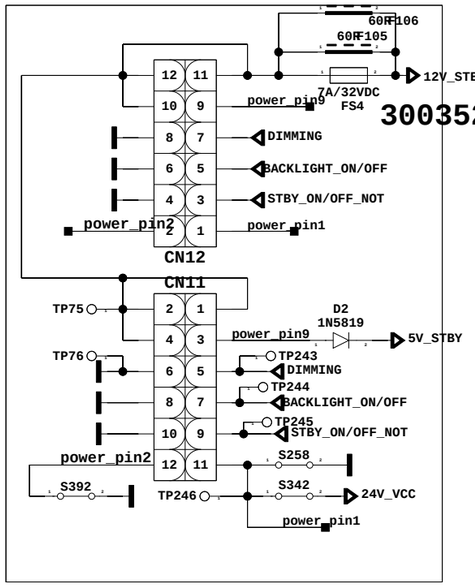






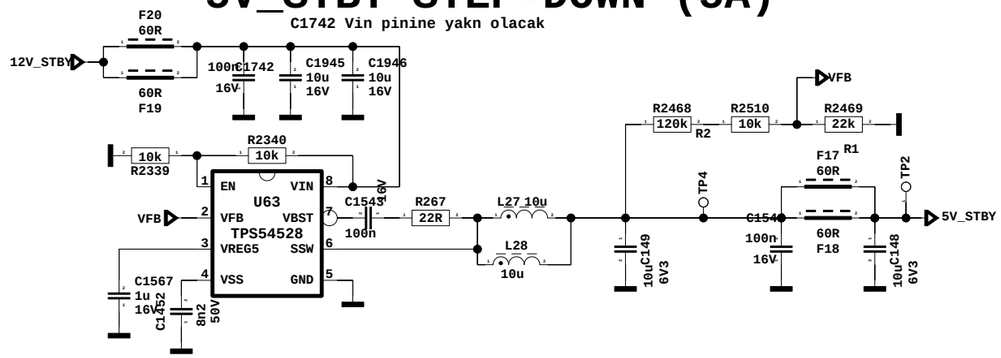


VESTEL	PROJECT NAME : 17mb230-r2	A3
	SCH NAME :AUDIO	T. SHT 15
	DRAWN BY :<YOUR NAME HERE>	14/03/2019:13:30

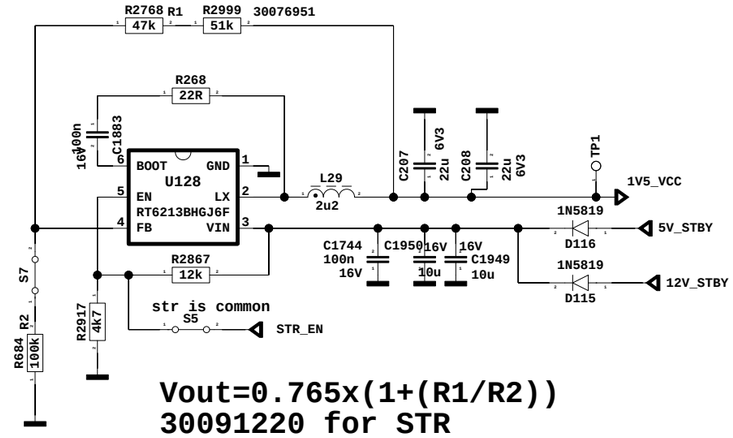


DC/DC 1
5V_STBY STEP-DOWN (5A)

C1742 Vin pinine yakn olacak

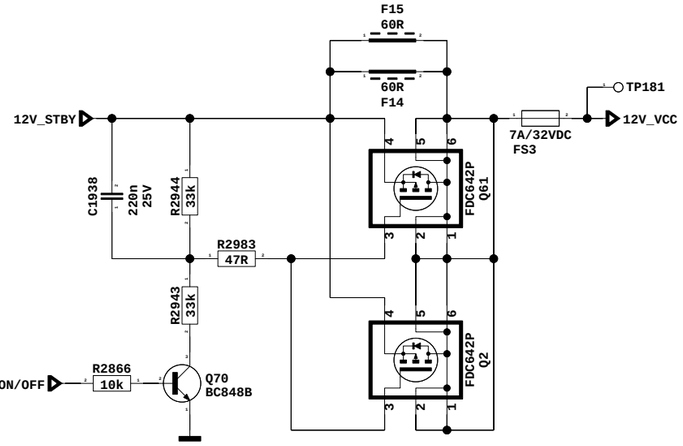


DC/DC 3
1V5_VCC DC/DC (2A)

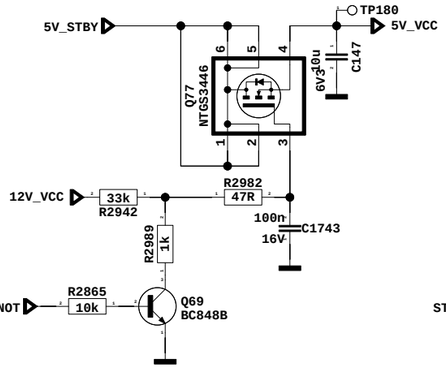


Vout=0.765x(1+(R1/R2))
30091220 for STR

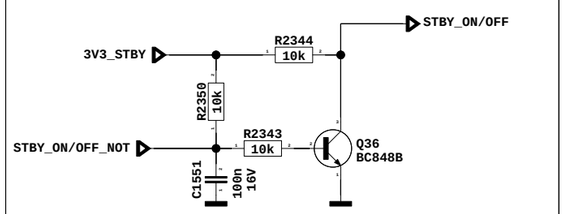
SW1
12V_VCC SWITCH



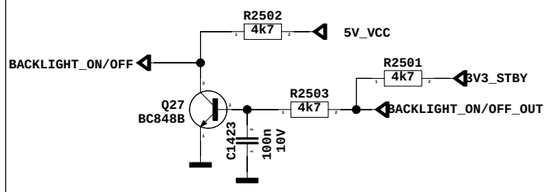
SW2
5V_VCC SWITCH



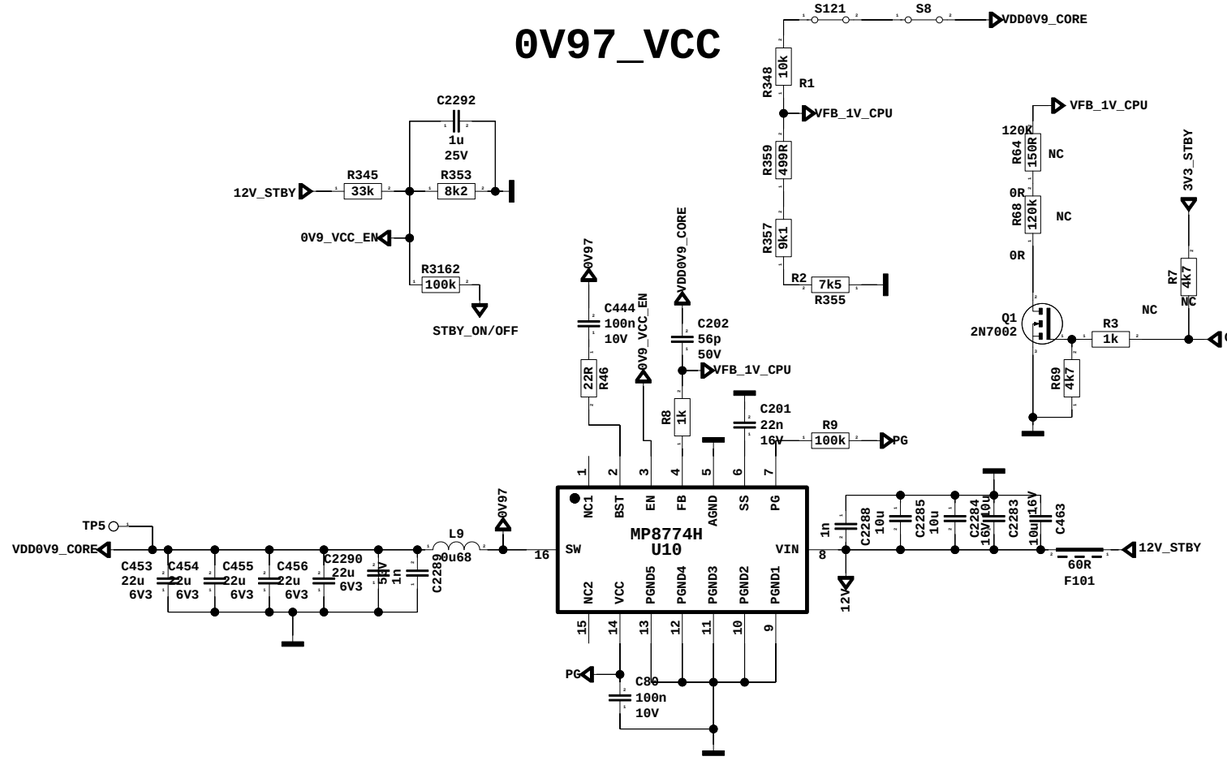
STBY On/Off Circuit



Backlight On/Off Circuit



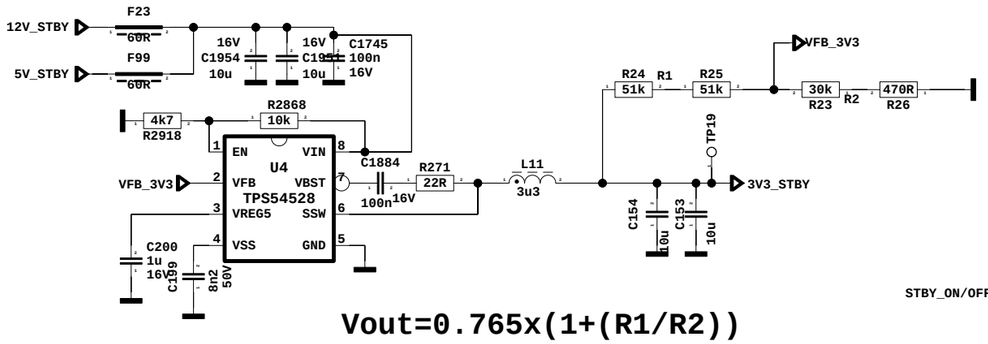
0V97_VCC



Vout=0.6x(1+(R1/R2))
R1=20k R2=30k Vout=1V

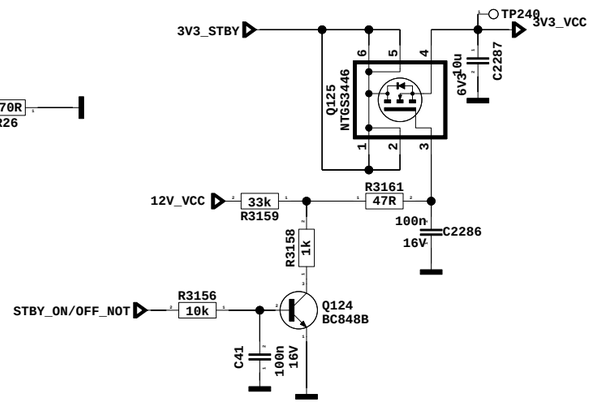
VESTEL	PROJECT NAME : 17mb230-r2	A3
SCH NAME :POWER	T. SHT	15
DRAWN BY :<YOUR NAME HERE>	26/03/2019:14:28	

DC/DC 2
3V3_STBY STEP-DOWN (5A)

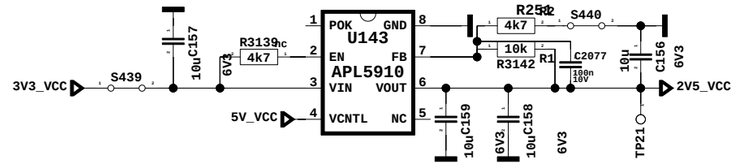


Vout=0.765x(1+(R1/R2))

SW3 3V3_VCC SWITCH



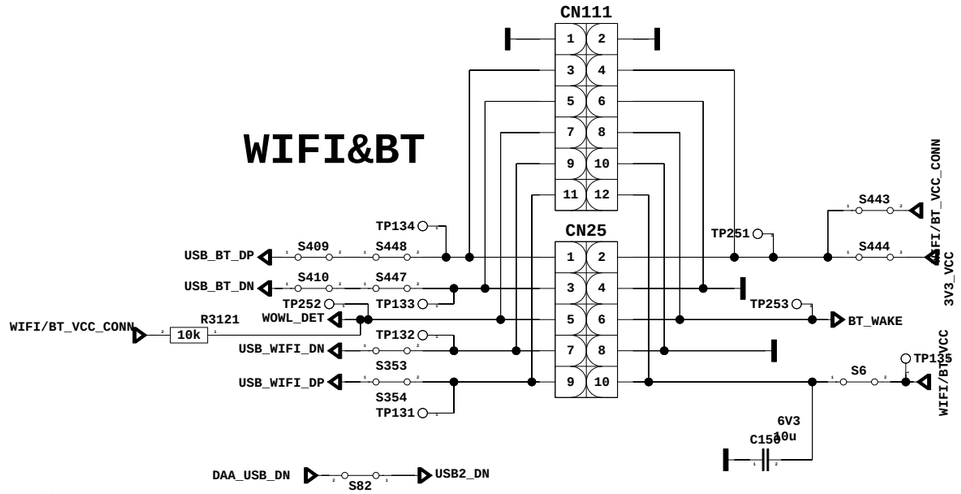
2V5_VCC LDO



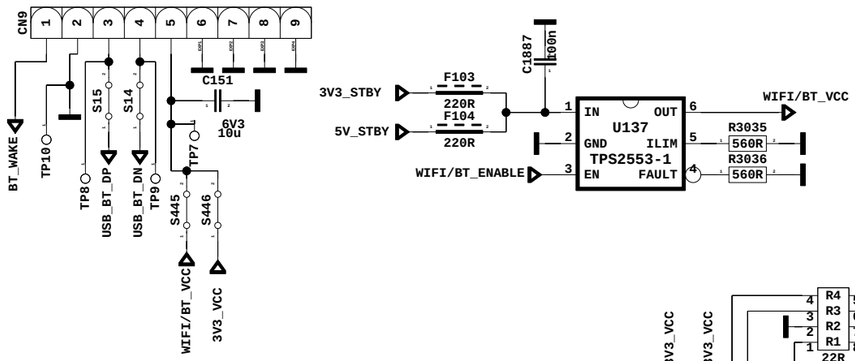
22ohms

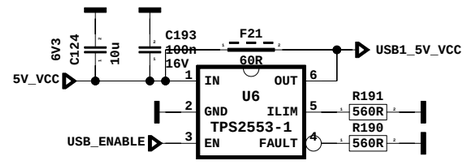
VESTEL	PROJECT NAME : 17mb230-r2 — A3
SCH NAME :POWER2	T. SHT 15
DRAWN BY :<YOUR NAME HERE>	11/03/2019:14:09

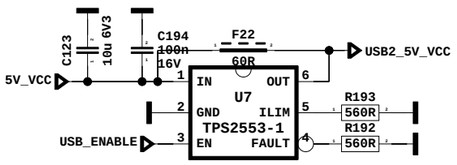
WIFI&BT

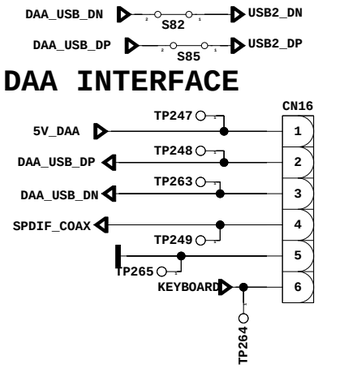


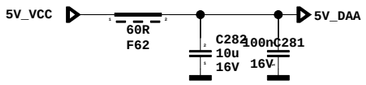
B2B BT



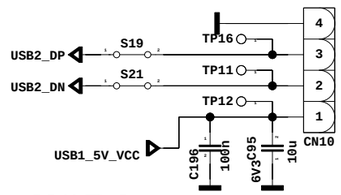




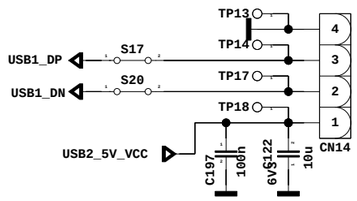


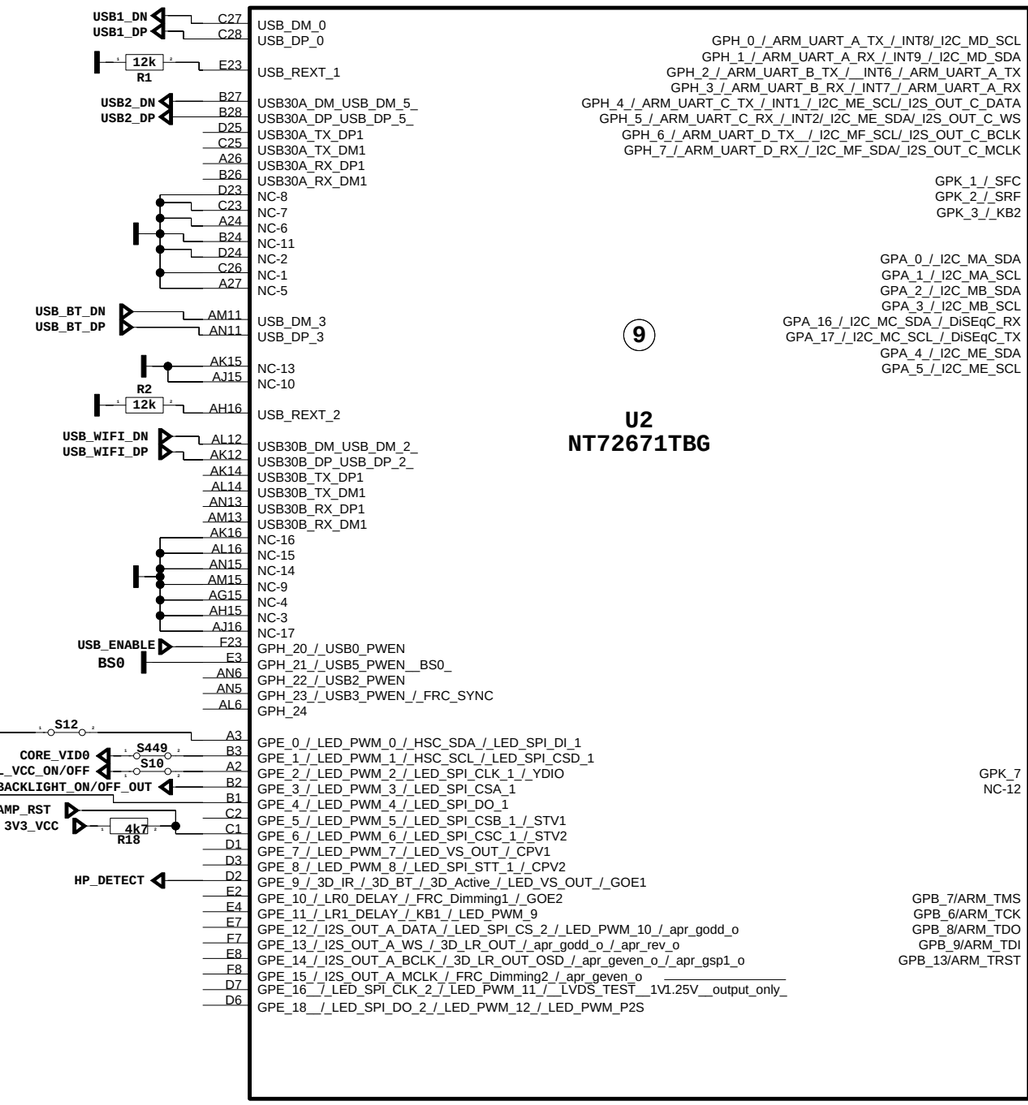


USB2

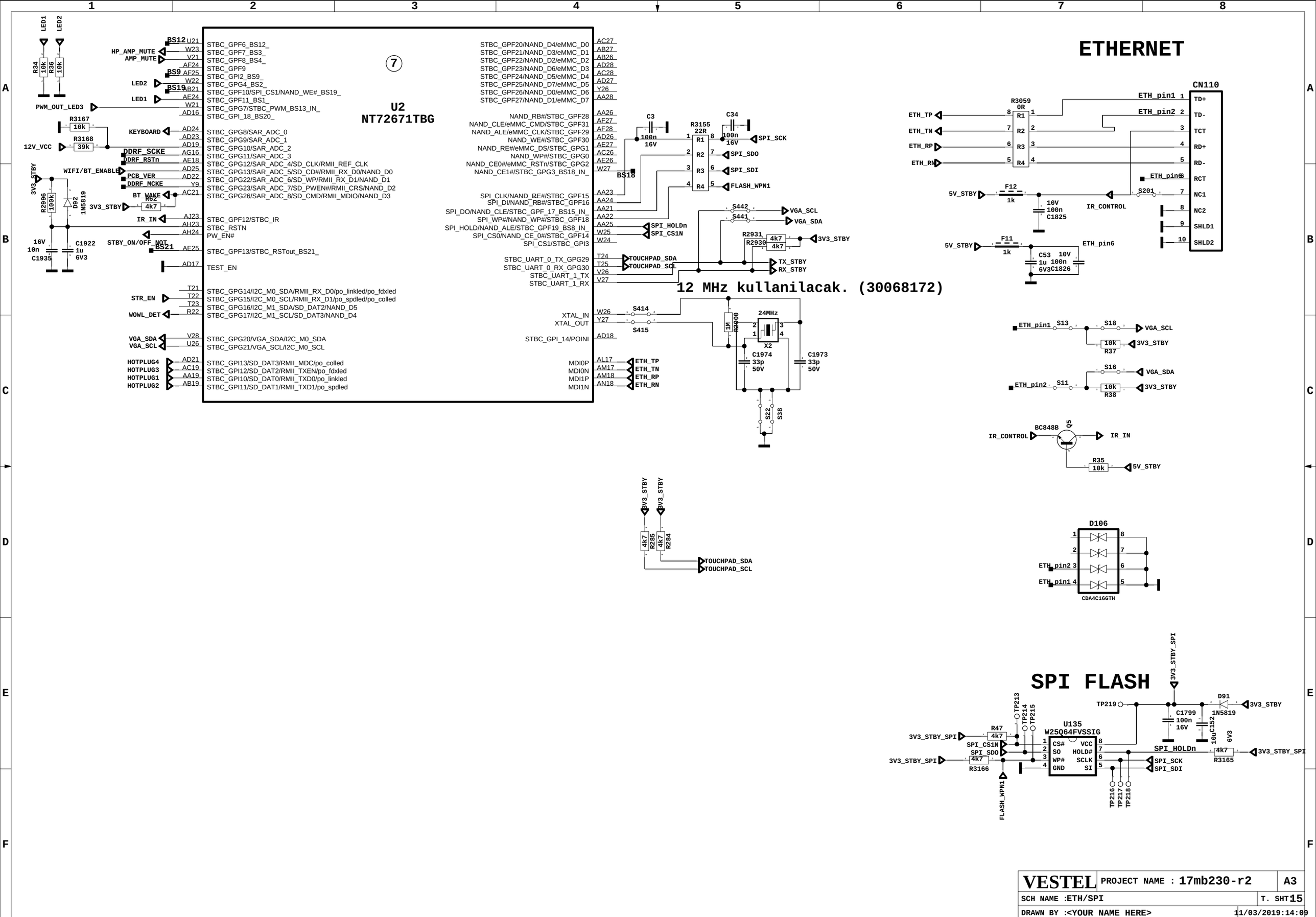


USB1





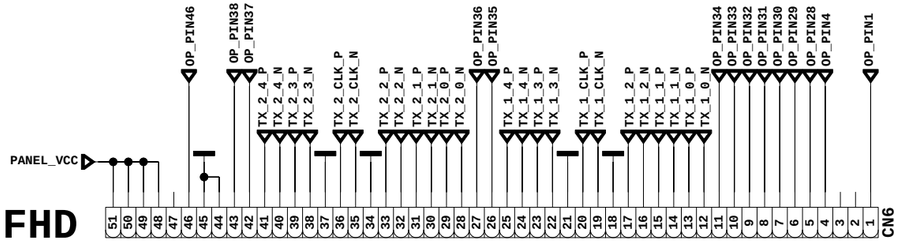
VESTEL	PROJECT NAME : 17mb230-r2		A3
SCH NAME :WIFI/USB		T. SHT	15
DRAWN BY :<YOUR NAME HERE>		19/03/2019:13:27	



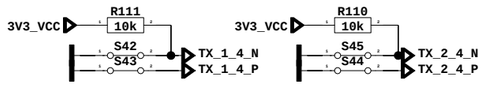
4,7Kohms

VESTEL	PROJECT NAME : 17mb230-r2	A3
SCH NAME :ETH/SPI	T. SHT	15
DRAWN BY :<YOUR NAME HERE>	11/03/2019:14:09	

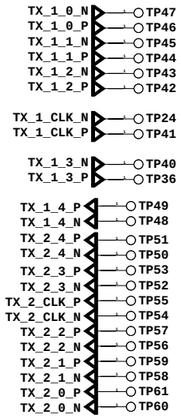
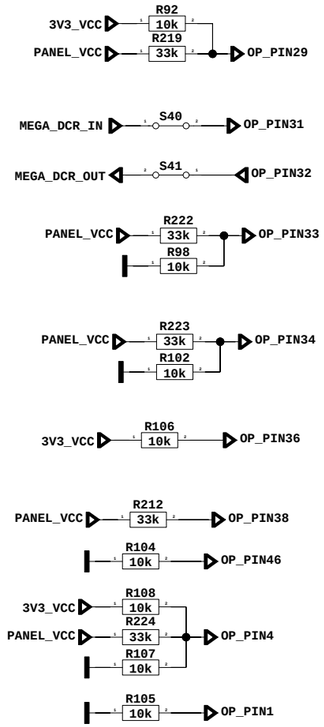
51 PIN FHD



10_BIT PANEL



Test Pins



OPTIONS TABLE